Impedance Source Converters for Renewable Energy Systems

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IMPEDANCE SOURCE CONVERTERS FOR RENEWABLE ENERGY SYSTEMS

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Impedance Source Converters for Renewable Energy Systems

Ph.D. Dissertation

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Abstract

Impedance-source networks are promising power conversion stages due to their performance in terms of flexible step-up/down conversion ratios, and high reliability with the shoot-through protection. Accordingly, significant efforts have been made to advance the impedance source converters through topological innovations, but there are still many limitations, which hinder their further applications in renewable energy systems.

In general, the impedance source networks can be integrated into the traditional voltage-source inverter, which makes it a single-stage solution with boost capabilities. Alternatively, they can be applied as the first-stage DC-DC converter in the two-stage power conversion solutions. However, such impedance source networks, have several disadvantages, e.g., a low voltage gain, a discontinuous input current, a narrow adjustable control range, and high voltage stresses across the components. If these problems cannot be effectively addressed, they will degrade the performance of the impedance source networks. Thus, the solutions to the above limitations are demanded. Additionally, although many efforts have been made to improve the performance of the impedance source networks through novel topologies, the design and optimization of the impedance source networks have not been fully addressed yet. Seen from the design perspective, the performance of the impedance source networks can be further enhanced. Therefore, it is necessary to demonstrate special design considerations and a systematic design procedure for impedance source networks.

With the above and in order to improve the integration of renewable energy systems with impedance source networks, this Ph.D. project was carried out to develop novel impedance source networks for high-efficiency and high-reliability DC-AC and DC-DC power conversion systems. Throughout this project, several impedance source networks are proposed, which can be employed in DC-AC and DC-DC conversion systems.

Compared with traditional impedance source networks, the proposed inverters based on the non-magnetic-coupled impedance networks can achieve a continuous input current, lower voltage stresses, and fault-tolerant operations. In addition, modified magnetic-coupled-based impedance source DC-DC con-

verters are proposed, which feature a continuous input current, trans-inverse capability, and a wide adjustable duty cycle range. Especially, the possible DC current saturation in the core is addressed by the configuration of the proposed magnetic-coupled-based topologies. To demonstrate the performance of the proposed topologies, benchmarking studies of the proposed topologies against several selected prior-art topologies in terms of voltage stress, input current ripple, component count, duty cycle control range. Lab-scale prototypes have also been built to validate the performance.

Furthermore, a systematic design method for impedance source networks was introduced in this Ph.D. project. Several specific design considerations in terms of topology, modulation strategy, switching frequency, and practical layout are explored. Additionally, the basic design principle is provided for capacitors and inductors, which are widely used in impedance-source converters. Moreover, the design procedure is demonstrated on a quasi-Z-source network design. An optimal design of the coupled inductors with different winding structures is also provided.

The contributions of this Ph.D. project have been presented in five journal papers and four conference papers.

Resumé

Impedans-netværk er lovende effektomformningstrinet i effektelektroniske apparater på grund af deres fleksibilitet til at kunne forøge eller reducere spændingen og havende en høj pålidelighed på grund af beskyttelse mod kortslutning i kredsen. Der er gjort en betydelig indsats for at fremme impedans-netværk omformerne via udvikling af nye topologier, men der er stadig mange begrænsninger, som hindrer deres anvendelser i eksempelvis vedvarende energisystemer såsom solceller, brændselsceller.

Generelt kan impedans-netværk integreres i den traditionelle effekt-omformer, hvilket muliggør en en-trins omformer-løsning, der kan forøge spændingen og samtidig tilsluttes nettet. Alternativt kan impedans-netværk anvendes i en DC-DC omformer som det første trin af en to-trins effektelektronisk omformer. Imidlertid har sådanne impedans-netværk omformere adskillige ulemper, såsom lille spændings-forstærkning, en diskontinuerlig indgangsstrøm, et lille justerbart reguleringsområde og høje spændinger over komponenterne med deraf tab til følge. Hvis disse problemer ikke kan løses effektivt vil de forringe ydeevnen af impedans-netværk omformerne og der behøves nye løsninger. Selvom der er gjort mange bestræbelser på at forbedre ydeevnen af dette ved nye topologier, er deres design og optimering endnu ikke blevet adresseret fuldt ud. Også set fra et design perspektiv kan ydeevnen af impedanskilde-netværk baserede omformerne forbedres yderligere. Det er også nødvendigt at undersøge nye design og udvikle en systematisk design-procedure for impedans-netværkene.

Med ovennævnte problemstillinger og for at forbedre integrationen af vedvarende energisystemer med impedans-netværk omformere, er dette Ph.D. projekt blevet udført med henblik på at udvikle nye impedans-netværk, som har en høj virkningsgrad og en høj pålidelighed der kan anvendes i både DC-AC og DC-DC omformere. Projektet foreslår adskillige nye impedans-netværk omformere.

Sammenlignet med traditionelle impedans-netværk omformer topologier kan de foreslåede invertere, der er baseret på ikke magnetisk koblede impedansn-etværk, opnå en kontinuerlig indgangsstrøm, have lavere spændinger over komponenterne og have en fejltolerant opførsel. Derudover foreslås mod-

ificerede magnetisk-koblede impedans-netværk DC-DC-konvertere, som har en kontinuerlig indgangsstrøm og et bredt justerbart drifts-område. Især adresseres en potentiel mætning af den magnetiske kerne ved brug af de foreslåede magnetisk-koblede topologier. For at demonstrere ydeevnen af de foreslåede topologier laves en benchmarking mod andre udvalgte topologier med hensyn til over-spænding, indgangsstrøm, antal brugte komponenter og arbejds-område, hvor de er kontrollerbare. Forskellige prototyper er opbygget i laboratoriet for at eftervise ydelsen af omformerne.

En systematisk design-metode til impedans-netværk omformerne er også introduceret i dette ph.d. projekt. Flere specifikke designovervejelser med hensyn til topologi, modulationsstrategi, switch-frekvens og praktisk layout er undersøgt. Derudover er tilvejebragt grundlæggende designprincipper til kondensatorer og induktorer, der ofte bruges i impedans-netværk konvertere. Designproceduren er demonstreret på en speciel impedans-netværk topologi og et optimalt design af de koblede induktorer med forskellige viklingsstrukturer er også tilvejebragt.

Bidragene fra dette ph.d. projekt er blevet præsenteret i fem tidsskrifts-artikler og fire konference-artikler.

Preface

This Ph.D. thesis is written according to the Ph.D. project entitled "Impedance Source Converters for Renewable Energy Systems". This Ph.D. project is supported by the Department of Energy Technology, Aalborg University, Denmark. In addition, I would like to express my acknowledgments to the Center Of Reliable Power Electronics (CORPE) and Otto Mønsteds Fond, who support me for the experimental equipment and conference participation during my entire Ph.D. study.

First of all, I would like to extend my deepest gratefulness to my supervisor Professor Frede Blaabjerg for his professional, kindness and patient guidance during the Ph.D. project period. His erudition, enthusiasm and hearty talks drives me to complete my Ph.D. study and I do believe that my future academic career and even my future life will benefit from what I have learned from Professor Frede Blaabjerg. Moreover, I would like to thank my co-supervisor Associate Professor Yongheng Yang for his advice, guidance and encouragement during the entire period of the Ph.D. project.

I am also grateful to Assistant Professor Minjie Chen for providing me an opportunity to visit Princeton University during my study abroad and broaden my knowledge in the area of the logic circuit and high-frequency converter design. Also, I would like to thank my all colleagues at Princeton University for their valuable help and great hospitality during my stay.

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Last but not least, I would like to express my sincere gratitude to my wife Ms. Guojin Zhang for her warm support during the whole period of my Ph.D. study. I also want to thank my family for providing me the greatest support in everything I do along with my entire study period.

Jing Yuan
Aalborg University, August 10, 2020

Contents

Report

Chapter 1

1 Introduction

This chapter presents the background and motivation of the Ph.D. project. The research questions and objectives are discussed. Then, the outline of the Ph.D. thesis is presented to show the flow of this research work.

1.1 Background

The shortage of fossil fuels, as the most widely used energy source, leads to significant emissions of greenhouse gases that bring out global warming. Moreover, fossil fuel-based transportation and further industrialization result in severe air pollution. To address these issues, renewable energy sources as a promising substitute for power generations have been increasingly developed in the past decades, as depicted in Fig. 1.1. Accordingly, the percentage of the renewable sources of the global generation power capacity has increased to above 33% in 2018 [1]. Compared with traditional fossil fuels, renewable energy features environmental-friendly, which can generate energy without any greenhouse gas emissions and help to reduce air pollution to some extent.

It is noteworthy that solar and wind energy have a rapid development compared with other types of renewable energy in the past years, which is presented in Fig. 1.2, where it can be seen that around 55% and 28% of the new renewable additions are solar photovoltaics (PV) and wind power [1]. However, the DC output voltages from the solar PV and fuel cells are normally low and variable due to the energy resource intermittency (i.e., the energy production is dependent on the operating environmental conditions like solar irradiance level). As a consequence, the power delivery from the renewable energies side to the grid/load side cannot be directly attained and power electronic converters are installed to solve this as interfaces. Thus, power electronic converters should be able to flexibly condition the voltage, effectively perform the power conversion, and accurately ensure a balanced power flow. The power electronic converters, as a critical connection between the renewable energy and the grid/load side, can have a major impact on

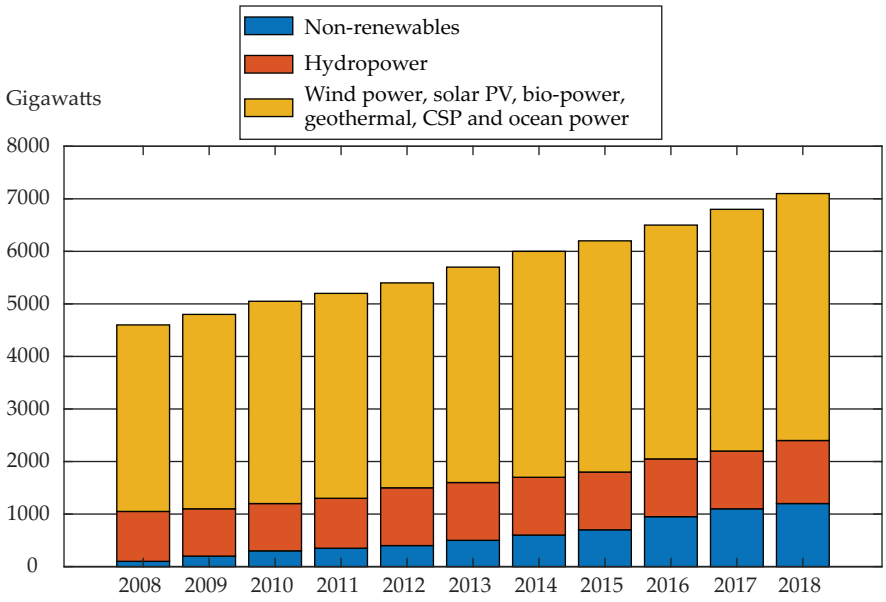


Fig. 1.1: Global power generating capacity from 2008 to 2018 [1].

the overall system performance with regard to stability, reliability, efficiency, power quality and energy utilization rate. With the renewable energies being increasingly adopted in practice, a variety of novel power converter topologies are introduced to guarantee a cost-effective energy conversion. This has also been driven by the continuously declining price of solar PV modules and the increasing demand for grid-friendly, green, and sustainable energy conversion systems.

Fig. 1.3 shows a general structure to integrate renewable power by using power electronics. In order to integrate the renewable energies into the power grid, the necessary power converters are utilized. That is, the power electronic systems should coordinate the outputs of renewable energy based on the demand of the power grid. Hence, the performance of converters has been significantly enhanced. This can be done either through topological innovations (i.e., novel power converter topologies) or by applying advanced control strategies. In this Ph.D. thesis, the focus will be on the development of novel power converter topologies. Furthermore, the converters for renewable source systems can be classified as galvanic-isolated and non-isolated ones [C1], [2]. According to the topologies proposed in [3–6], the isolated converters, also known as transformer-based converters, feature high boosting capability by applying a transformer to separate the input and output. However, the extra transformers may result in high cost, large size and low efficiency (i.e., transformerless solutions) compared to their counterparts as claimed by

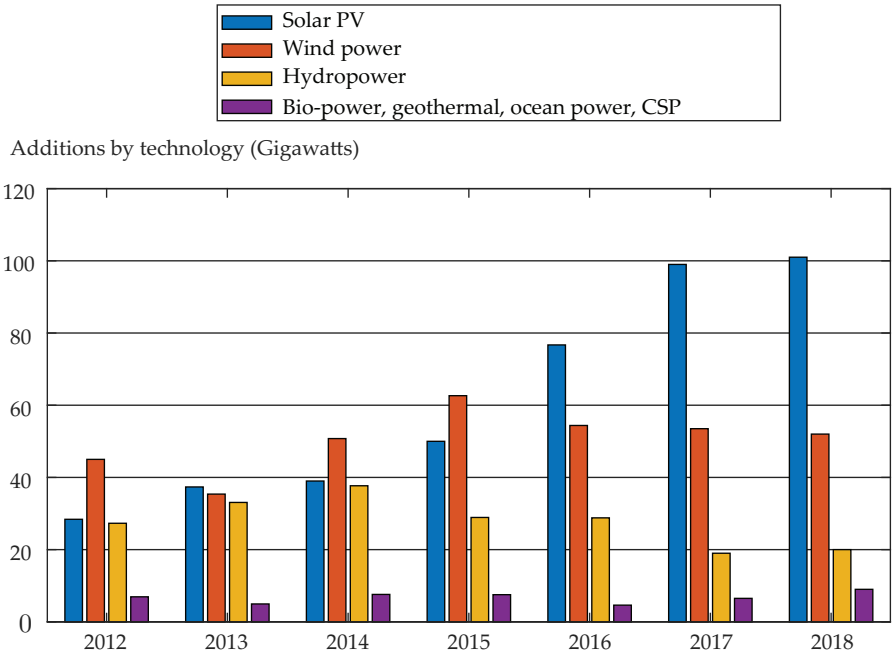


Fig. 1.2: Annual additions of renewable power capacity from 2012 to 2018 [1].

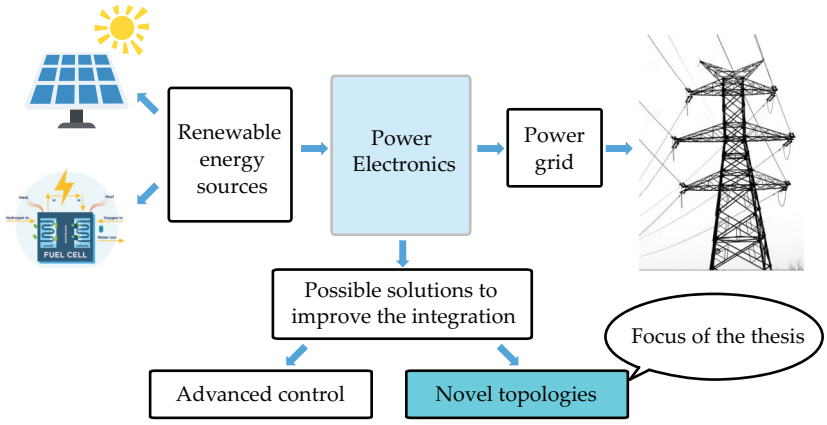


Fig. 1.3: The general structure to integrate renewable power generation using power electronics.

the demonstrations in [7, 8]. Hence, the non-isolated converters hold more promise in the power conversion process considering all aspects.

- Two-Stage Non-Isolated Solutions

  In a traditional two-stage power conversion solution, the first stage usually applies the boost converters. For example, in the PV applications, the input voltage is boosted to a requirement level while the converter tracks the maximum power point of the solar power [2, 9]. Furthermore, the second DC-AC stage is used to invert the DC voltage to AC voltage [C1], [2]. Meanwhile, the AC current can be injected into the grid [10, 11]. Although the boost converters can be employed to enhance the input voltage during the first stage, basic boost converters are not suitable for the applications where high voltage gains are required. Consequently, the extra inductors or capacitors can be implemented into the basic boost converter for higher boosting capability [10–12]. Additionally, the boosting capability can be further improved by adding coupled inductors to the networks. Although they can provide high conversion ratios by adjusting the turns-ratios, the unexpected leakage inductance may degrade the performance concerning the efficiency and power density.

- Single-Stage Non-Isolated Solutions

  In the last decade, the research trend was to reduce the number of components, by means of a single-stage conversion. The pseudo-DC-link topology is one of the milestones aiming to reduce conversion stages and simplify the topology [2]. In addition, several single-stage buck-boost topologies have been proposed [7]. It should be noted that these proposed topologies can be obtained by reconfiguration the basic buck-boost network [13]. Similarly, the switched-inductor could be utilized to replace the basic inductor for a higher voltage gain [14]. Moreover, the single-stage topologies can apply the coupled-inductors to reduce the component count [15, 16].

In fact, the above-mentioned two solutions are both extensively applied in practical applications due to their certain characteristics. For the two-stage solutions, the boosting-stage and inverting-stage can be separately optimized. Especially in the PV systems, the DC-link capacitor is used to buffer the double-line-frequency (DLF) voltage ripples [C1], [2]. However, if the DLF voltage ripples are eliminated by single-stage solutions, larger electrolytic capacitors must be placed near the PV panels. However, capacitors may lead to failure considering the possible harsh environment conditions [2]. Moreover, compared to single-stage solutions, the two-stage solutions may have a lower efficiency owing to the losses in two stages. Meanwhile, the entire cost is also increased, considering its high component counts. Therefore, some research has been performed to enhance the performance of the two-stage and single-stage solutions through topological innovations. Especially, impedance-source

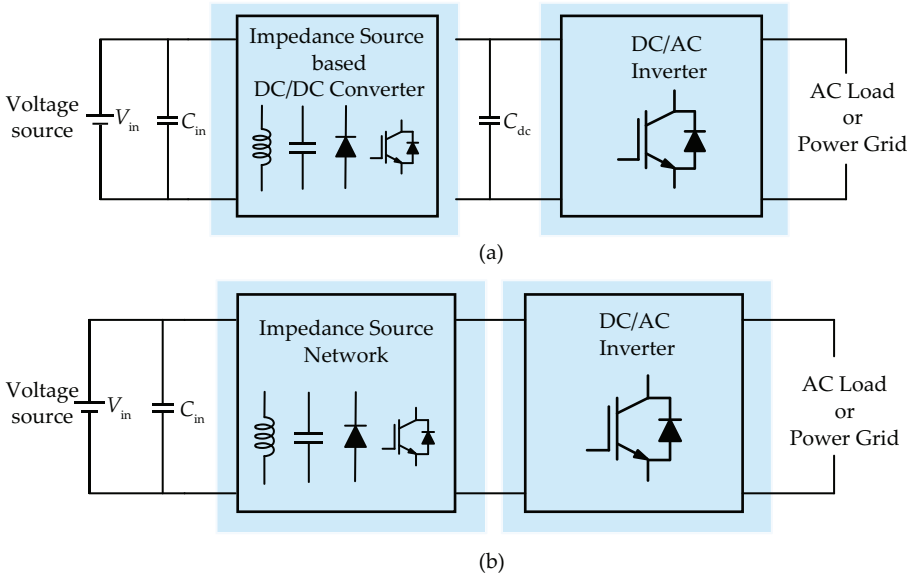


Fig. 1.4: Conversion stages diagrams based on impedance-source network: (a) two-stage solution, and (b) single-stage solution. (C_{in} and C_{dc} represent input capacitor and dc-link capacitor)

networks (ISN) have been increasingly discussed and provided an efficient solution for power conversion stages due to their extraordinary performance in terms of flexible step-up/down conversion ratios, and high reliability due to the shoot-through protection ability. ISNs can be applied as the first-stage DC-DC converter in the two-stage solutions. Additionally, ISNs are integrated into the traditional voltage-source inverter, which makes it be operated in the single-stage solution with buck-boost capabilities. Fig. 1.4 presents the conversion stages principles for two-stage and single-stage solutions with ISNs. The development of ISNs will be discussed as follows.

1.2 Impedance-Source Networks Development

It is common knowledge that the voltage-source inverter (VSI) cannot boost source voltages due to its buck characteristics [17]. Therefore, the above-mentioned boost converter is necessary for the expected boosting capability, which results in higher cost and lower efficiency. Moreover, the power switch failures may happen when the switches on the same inverter bridge turn on simultaneously due to unexpected gating signals. In the worst cases, the entire power supply has to be ceased, which further leads to loss of energy generation and incurs more investment. In order to tackle the above-mentioned drawbacks of the conventional VSI, the basic IS converter, also called Z-source inverter (ZSI), was introduced in [18]. The originally invented

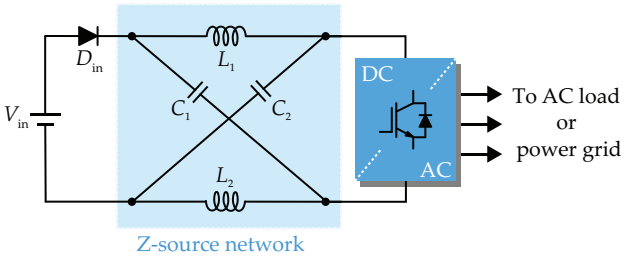


Fig. 1.5: Schematic of the Z-source inverter (ZSI) [18], where V_{in} is the input voltage.

ZSI includes two inductors, two capacitors, and a conventional two-level VSI, as it can be seen in Fig. 1.5. This basic ZSI features buck-boost capability and can be used in the single-stage power conversion [17]. In addition to applying ISNs to the DC-AC conversion, the impedance-source concept could extensively be employed in DC-DC, AC-DC and AC-AC power conversion [19, 20].

1.2.1 Operation Principle of the Impedance-Source Inverter

The operation principles of all kinds of IS converters are similar. Therefore, the basic ZSI is exemplified to demonstrate the operation principle. The schematic of the ZSI and its equivalent circuits under the shoot-through (ST) state and non-shoot-through (NST) state are presented in Fig. 1.6 [18]. During the ST stage (short-circuiting the inverter legs), as demonstrated in Fig. 1.6(a), inductors L_1 and L_2 store the energies from capacitors C_1 and C_2, and the diode D_{in} is OFF-state [18]. During the NST stage, the ZSI operates as the traditional VSI does. The diode is in conduction mode and the inductor releases the reserved energies via the VSI, and then, transferring the energy to an AC load or grid, as observed in Fig. 1.6(b). In contrast to the traditional VSI, the ZSI can achieve a buck-boost capability by regulating the duty cycle of the ST state in one switching period.

1.2.2 Development of Impedance-Source Converters

Since the ZSI is firstly introduced by Prof. F. Z. Peng [18], an increasing number of ISNs are developed during the last decade for improved performance. The general demands to such ISNs are to obtain a high boosting capability, continuous input current, low voltage stresses, high efficiency and reliability [J1], [21].

Especially for the low voltage renewable sources (e.g., fuel cells and solar panels), the voltage gains of a traditional DC-DC converter and ZSI are limited due to the need for an extreme duty cycle, so they cannot provide the required power with high conversion ratios. Moreover, the effective utilization

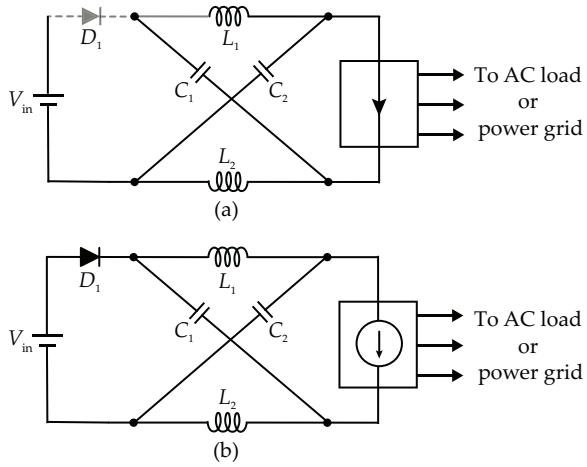


Fig. 1.6: Equivalent circuits of the Z-source inverter: (a) shoot-through state, and (b) non-shoot-through state [18].

of renewable energies mainly depends on the input current characteristic. For instance, in [22], it is validated that more fuel should be used if the input current has high ripples. Similarly, the power converters applied in the PV systems prefer achieving the continuous input current to achieve an accurate maximum power point tracking (MPPT) [23]. Hence, the continuous characteristic of the input currents is critical to the performance of the converters, which may decrease the stress and extend the life of the input sources.

Generally, ISNs are classified into two categories: non-magnetic-based and magnetic-based. The non-magnetic-based impedance networks are mainly derived by two methods. One method is to integrate extra diodes and switches to the basic Z-source network (see Fig. 1.5). The other one is to rearrange the components for specific features and advantages. On the other hand, the magnetic-based topologies are developed by integrating coupled inductors or transformers to the impedance networks. The utilization of magnetic components can greatly reduce the component count compared with the non-magnetic-based topologies so that the power density is improved and the cost is saved to some extent [24]. However, the magnetic design is one of the concerns.

- Non-magnetic-based Impedance Network

The impedance networks without magnetic components are originally from the basic Z-source network. Although the ZSI features considerably high conversion ratio and inherent shoot-through protection abilities, certain issues like chopped input current and high voltage stress prevent it having more applications to some degree [C3], [25]. Then, it is observed in Fig. 1.7

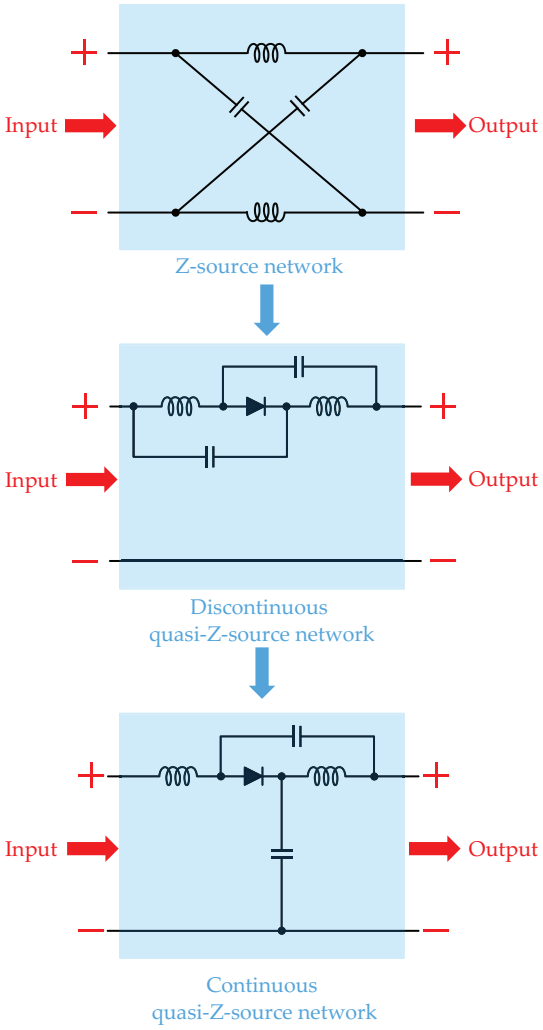


Fig. 1.7: Quasi Z-source networks with discontinuous and continuous input currents [26].

that the quasi Z-source inverter (qZSI) derived from the Z-source network was developed, which addresses the above restraints by rearranging the components [26]. Furthermore, more explorations based on the ZSI/qZSI have been presented in the prior-art topologies to improve the performance of the ISNs [27–36].

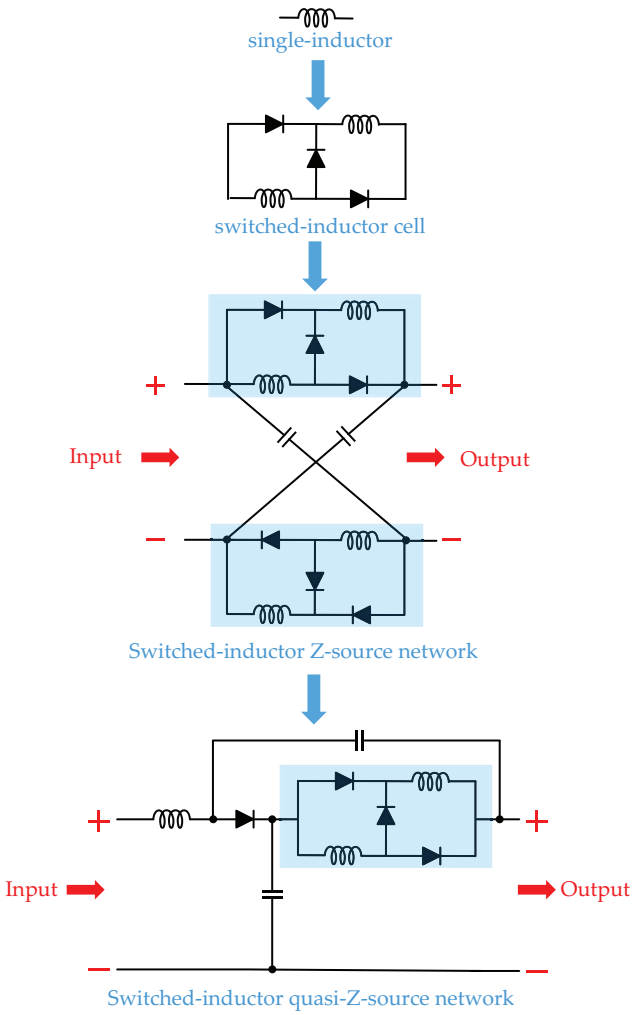


Fig. 1.8: Advanced Z-source networks using switched-inductors [27, 28].

Clearly, increasing the boosting capability can be achieved by adding more components to the basic impedance networks. By following this principle, the switched-inductor (SI) or switched-capacitor (SC) networks are employed as the substitutes of the inductors/capacitors in the ZSI/qZSI, thereby resulting in a higher boosting capability [27–36]. For example, it can be seen in Fig. 1.8 that the inductors in the ZSI/qZSI are substituted by two SI networks, where higher boosting ratios are obtained by employing a very small ST duty cycle [27, 28]. Moreover, the SI-qZSI could ensure continuous input as well as lower stresses in contrast to the SI-ZSI [27, 28]. In addition, the SI-qZSI could

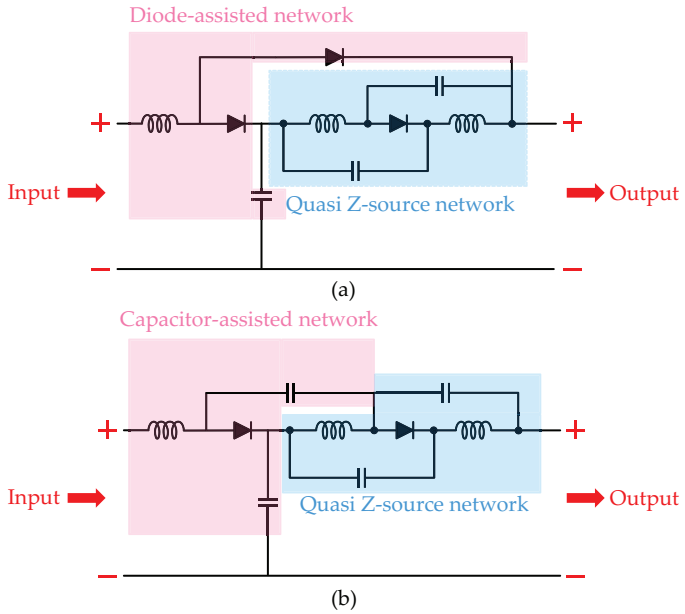


Fig. 1.9: Extended Z-source networks: (a) diode-assisted Z-source inverter, and (b) capacitor-assisted Z-source inverter [37].

suppress the starting current to a large extent, which protects the components effectively. In [29, 34], the input inductor is also replaced by an SI cell for a better boosting capability, lower stresses as well as higher efficiency. So as to further enhance the performance with respect to high stress and poor power quality caused by a low modulation index, generalized multicell SI/SC-ZSIs are proposed [30]. The proposed converters in [35, 36] utilize an SC network to achieve lower voltage stresses, smaller inductors, and higher voltage gain and efficiency. In addition to the topologies based on SI or SC networks, the ZSI/qZSI can be extended by integrating capacitors and diodes for higher boosting capability and lower voltage stress over the capacitors [37], as observed in Fig. 1.9. Although these converters based on SI, SC cells can tackle the limitations of the conventional ZSIs, they require lots of passive components, which may bring about some problems, such as high cost, large volume and low power density.

To address the above problems, several prior-art ZSI topologies with active switches were introduced [38–49]. The basic switched boost inverter (SBI) and quasi-SBI (q-SBI) are shown in Fig. 1.10. Compared with the ZSI/qZSI, the SBI and qSBI have fewer passive components, but achieves the same boosting capability with only one active switch [38, 39]. Nevertheless, the capacitor voltage stress is very high due to the parallel connection to sources.

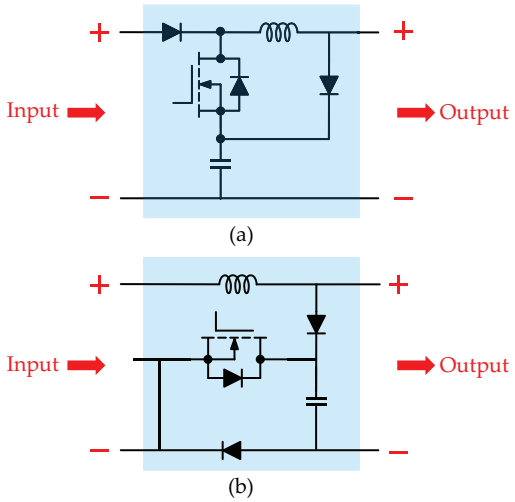


Fig. 1.10: Switched-based Z-source topologies: (a) switched boost inverter and (b) quasi-switched boost inverter [38, 39].

Furthermore, the input current is discontinuous because of the diode. The modified converters based on the SBI/qSBI in [40, 41, 44, 46–50] solve the aforementioned issues, where include active switched capacitors/inductors and an SBI/qSBI network. This kind of modified topologies normally have high step-up voltage gains and achieve lower voltage stress over the switches of the inverter legs without additional passive components. Moreover, another feature of this topology is that more SI/SC cells can be integrated into the circuit in a cascaded way for a higher boosting ratio [49]. In [43, 45], a common ground converter based on switched networks, SCs, and the qZSI was proposed by rearranging the layout of the main power switches. Additionally, the active switches in the proposed topology lead to a bidirectional converter, which makes it suitable to be applied in a hybrid energy sources system for electric vehicles.

Moreover, it is known that the input current of ZSIs is typically discontinuous because of the direct connection between the dc source and the input diode [51]. To tackle this, several embedded-ZSIs (E-ZSI) were proposed, which can guarantee continuous input currents [51–60]. The embedded concept was proposed by P. C. Loh et al. in [51], and its multisource structure is particularly appropriate for PV or fuel cell systems. The original asymmetrical and symmetrical embedded ZSIs (E-ZSI) are shown in Fig. 1.11, where we can see that the input sources, such as PV panels, are in the direct connection with the inductors of the basic ZSI in Fig. 1.5 [51]. In [52], the embedded topologies were proposed asymmetrically and symmetrically based on the input source locations. Especially, the desired requirement of the input current and voltage

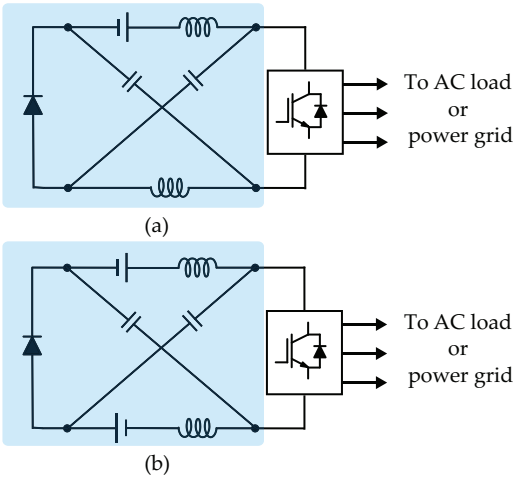


Fig. 1.11: Embedded Z-source inverters : (a) asymmetrical structure, and (b) symmetrical structure [51].

filtering can be achieved by arranging the source positions. Despite the fact that the above-reviewed embedded-ZSIs are able to overcome certain drawbacks of the traditional ZSIs, the boosting capability cannot be considerably improved. Therefore, the E-ZSI can also be extended by using SI/SC cells or extra active switches for a better boosting capability to be suitable for different applications.

- Magnetic-based Impedance Network

Coupled inductors and transformers are effective components to improve the performance of ISNs, where the conversion ratios are able to be enhanced without sacrificing the modulation index. Additionally, the number of passive components is greatly reduced by using coupled inductors or transformers. Therefore, the improved power density reduces the overall cost to some extent [19]. The T-source inverter (TSI), trans-ZSI and trans-qZSI are typical representatives of magnetic-coupled ZSIs, which are shown in Fig. 1.12 [61, 62]. They only utilize one coupled inductor with two windings as well as one capacitor. Voltage gains of the TSI and trans-qZSI are modulated by changing turns-ratios of the coupled inductor, and stresses across the switches can be reduced [61, 62]. Additionally, they share a common voltage source between the voltage source and the inverter, and thus electromagnetic compatibility issues in the ZSI can be potentially solved [61, 62]. Nonetheless, the leakage inductances of the coupled inductor must be low to prevent the overvoltages. In [63], the cascaded trans-ZSI uses several magnetic networks in an alternately cascaded structure to keep the currents and voltages stresses of the devices low.

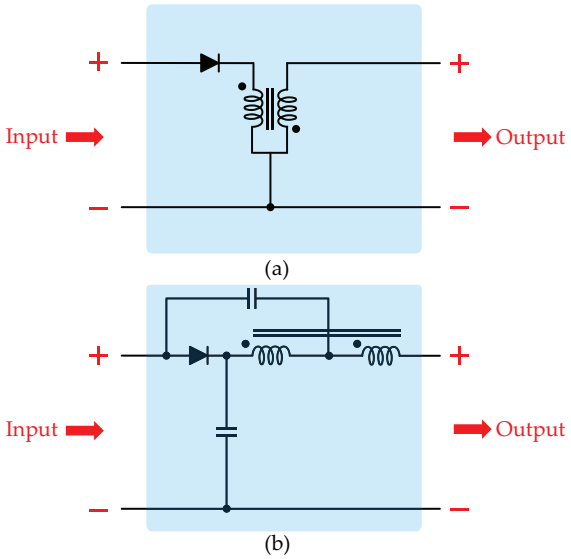


Fig. 1.12: Magnetic-coupled networks: (a) T-source inverter/trans-Z-source inverter, and (b) trans-quasi-Z-source inverter [61, 62].

Moreover, the proposed topology is modified by rearranging the components in the trans-ZSI, featuring a high boosting capability, continuous input current, and resonance suppression at startup [64]. By this modification, the improved trans-ZSI is very suitable for PV or fuel cell systems.

Furthermore, as indicated in Fig. 1.13 (a), the Γ-shape impedance network was proposed to enhance the boosting capability [65]. However, it can only draw a discontinuous input current. To tackle this, a modified Γ-shape topology was introduced in [66]. Another advantage of this modified Γ-ZSI is lower turns-ratios of the coupled inductor contributes to larger voltage gain, which reduces the cost compared with TSIs and trans-ZSIs [66]. In addition, in the proposed improved the Γ-ZSI [69], the transformer and inductor share the same core to obtain high conversion ratios and modulation index. The main advantages of this topology are that the core of the coupled inductor cannot be saturated compared with other similar topologies and high-frequency ripples from the input current can be filtered out [69].

In addition to the above topologies based on a two-winding structure, a three-windings Y-source converter (YSC) is introduced in [70], as shown in Fig. 1.14(a). This unique structure has one more degree of freedom in comparison to the above-discussed topologies, so that it can offer much flexibility to design the conversion gain. However, it suffers from the discontinuous input current and degraded performance due to the leakage inductance. To achieve continuous input currents, modified Y-source converters in Fig. 1.14(b) and

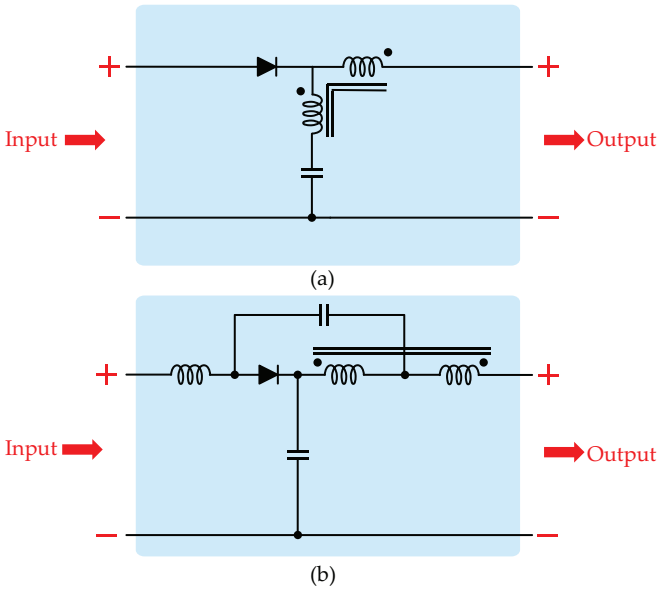


Fig. 1.13: Magnetic-coupled networks: (a) Γ-Z-source inverter [65], and (b) symmetrical Γ-Z-source inverter [66].

(c), were proposed, where the core saturation can be prevented with extra blocking capacitors [66, 68]. Moreover, as mentioned previously, the SC or SI cells can also be applied in the YSC [71] for a higher boosting ratio. Based on the Y-source concept, a Δ-source network was proposed [72]. In comparison to the YSC, the core size of the Δ-source network is optimized to a smaller one due to the lower magnetizing current [72]. Moreover, the adverse impact of leakage inductance on the converter performance is greatly reduced [72]. Nevertheless, the core losses of the Δ-source network are higher because of larger magnetizing current ripples.

1.3 Project Motivation

As discussed in the previous section, further attempts for IS converters should be made to improve the integration of renewable energy systems.

Firstly, the novel impedance-source topologies with high boosting capabilities can be achieved by rearrangements of the components based on the existing topologies. By changing the DC source positions, continuous input current can be achieved, and thus it is a promising candidate for sustainable energy utilization. Moreover, the resultant new topologies can allow the voltage stress across the components to be reduced, and the reliability of the converter could be improved compared with already existing topologies.

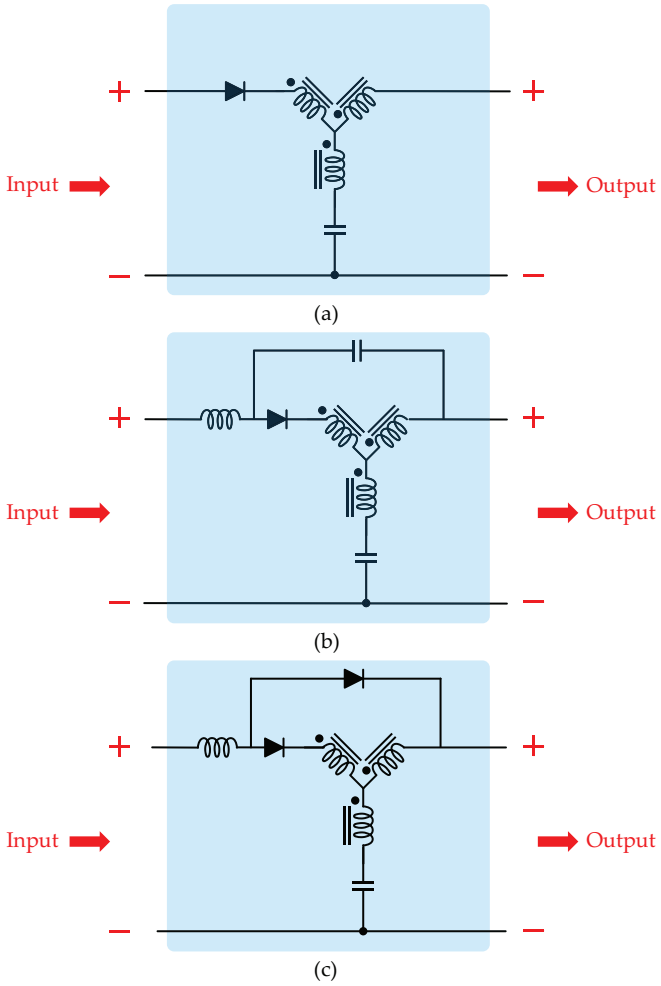


Fig. 1.14: Y-source networks: (a) basic Y-source network in [67], (b) modified Y-source network in [66], and (c) quasi-Y-source network in [68].

Secondly, the demand for low switch stresses and a wide adjustable control range in the coupled-inductor based DC-DC converters is of importance. By inserting the IS network to the existing DC-DC converters and changing the position of the components, more cost-effective topologies can be achieved.

Finally, in order to fill the design gap of the IS converters, a systematic design procedure to optimize the design of the components is highly required. This can be achieved by considering certain design considerations in terms of topologies, modulation strategies, switching frequencies and practical layout optimization.

1.4 Research Hypothesis and Objectives

1.4.1 Research Questions

The objective of this project is to develop new impedance-source networks for high-efficiency and high-reliability in DC-AC and DC-DC power conversion systems. As a result, the fundamental research hypothesis is considered:

- How to enable high-performance integration of renewable energy through developing novel impedance-source converters?

Thus, some subsequent research questions can be obtained as:

- What are the advantages of the proposed impedance-source topologies compared with the traditional Z-source topologies?
- Is it possible to develop a new impedance-source topology which enables high voltage gains and low voltage stresses across the components?
- Is it possible to apply impedance-source networks to the DC-DC converters with high boosting capabilities and a wide adjustable control range?
- How to conduct a systematic design and optimization for the impedance-source network?

1.4.2 Project Objectives

According to the above research questions, the objectives of this Ph.D. project are described as follow:

- **Development of novel impedance-source inverters:** Considering the limitations of the existing ZSIs, several modified ZSIs will be developed in this Ph.D. project. Compared with traditional ZSIs, the developed ZSIs should be designed to obtain continuous input currents, low voltage stresses, and fault-tolerant operations. The superior performance of the novel ZSIs should be validated through the experimental tests.
- **High-performance step-up DC-DC converter topologies:** As discussed previously, the existing topologies based on coupled inductors or transformers have certain drawbacks. To address this, novel impedance-source converters based on coupled-inductors will be developed in this Ph.D. project. New DC-DC converters are expected to achieve lower voltage stresses over the active switches and a wide adjustable control range. The prototypes should also be built to validate the performance.

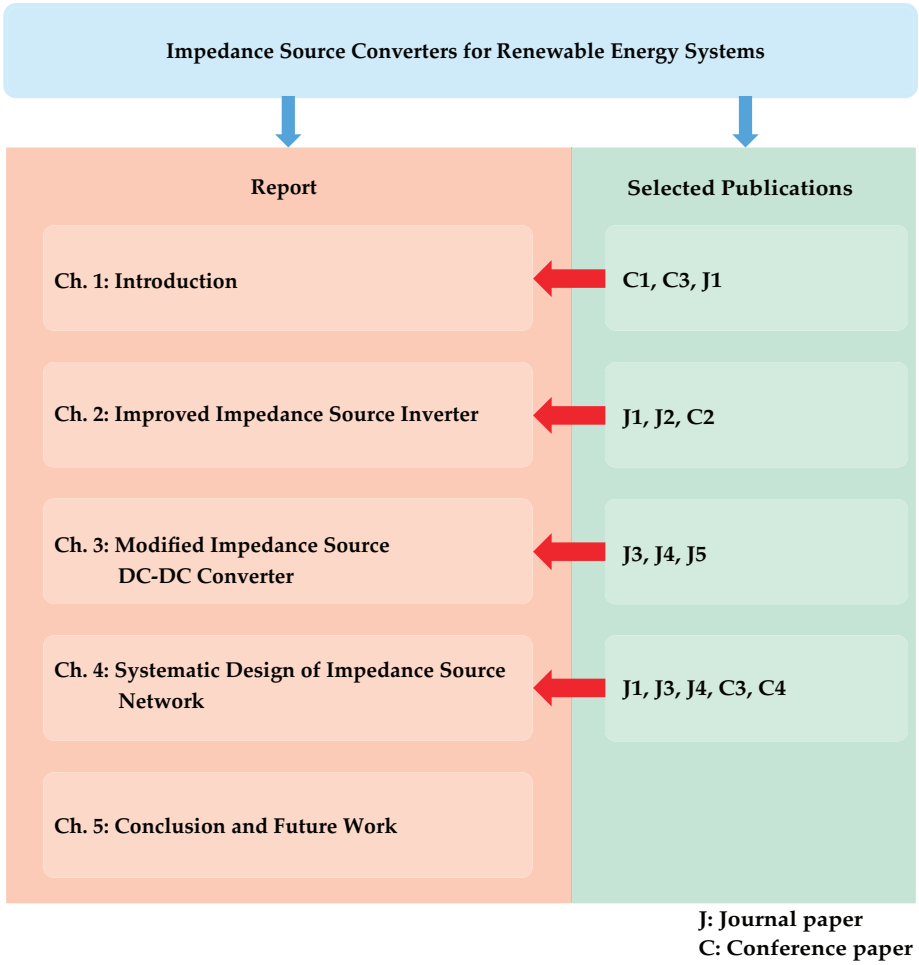


Fig. 1.15: Thesis structure and correlation between the report and selected publications.

- **Design and optimization of impedance-source network:** Although novel topologies are increasingly developed, the systematic design of impedance-source networks has not been fully addressed yet. Therefore, the last objective of this project is to introduce a systematic design procedure to optimize the design of the components. To maximize the performance of the IS networks, design principles in terms of topology selection, modulation selection, and switching frequency selection will be explored.

1.5 Thesis Outline

The obtained results and outcome of the Ph.D. project are documented in the Ph.D. thesis by collection of published papers. The thesis includes two main parts: the report and the selected publications, as illustrated in Fig. 1.15. The report gives a brief summary of the research outcome related to this project, while the selected publications present the paper outcome obtained during the Ph.D. study period.

The report begins with the introduction of the Ph.D. project by presenting the background, state-of-the-art, research questions, and project objectives. *Chapter 2* introduces single-stage DC-AC inverter topologies by applying IS networks. The topologies can be classified as switched-inductor based, switched-capacitor based and active switched based. The detailed analysis of the proposed ZSIs and experimental verification is also demonstrated in this chapter. In *Chapter 3*, the proposed DC-DC converters based on coupled inductors are presented for renewable energy applications; especially, the operation principle, benchmarking of the various DC-DC converters, and the experimental verification of the proposed converters are presented. Next, in *Chapter 4*, a systematic design procedure of the impedance-source converters are presented by case studies. Finally, *Chapter 5* concludes the thesis, and the main contributions of the Ph.D. study are summarized and the future research perspectives are outlined.

1.6 List of Publications

The research outcomes from the Ph.D. project have been disseminated in the forms of publications: journal papers, conference publications, as listed below. Some selected papers are summarized and used in the Ph.D. dissertation as previously listed.

Journal Papers

J1. **J. Yuan**, Y. Yang, P. Liu, Y. Shen, and F. Blaabjerg, "Modified Impedance-Source Inverter with Continuous Input Currents and Fault-Tolerant Operations" *Energies*, vol. 13, no. 13, pp. 3408, Jul. 2020.

J2. **J. Yuan**, Y. Yang, and F. Blaabjerg, "A Switched-Quasi-Z-Source Inverter with Continuous Input Currents" *Energies*, vol. 13, no. 6, pp. 1390, Mar. 2020.

J3. **J. Yuan**, A. Mostaan, Y. Yang, Y. P. Siwakoti, and F. Blaabjerg, "A Modified Y-Source DC/DC Converter with High Voltage-Gains and Low Switch Stresses" *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7716-7720, Aug. 2020.

J4. A. Mostaan, **J. Yuan**, Y. P. Siwakoti, S. Esmaeili, and F. Blaabjerg, "A Trans-Inverse Coupled-Inductor Semi-SEPIC DC/DC Converter with Full Control Range" *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10398-10402, Nov. 2019.

J5. F.A.A. Meinagh, **J. Yuan**, and Y. Yang, "Analysis and Design of a High Voltage Gain Quasi-Z-Source DC-DC Converter" *IET Power Electron.*, vol. 13, no. 9, pp. 1837-1847, Jul. 2020.

Conference Papers

C1. **J. Yuan**, F. Blaabjerg, Y. Yang, A. Sangwongwanich, and Y. Shen, "An Overview of Photovoltaic Microinverters: Topology, Efficiency, and Reliability" in *Proc. CPE-POWERENG*, pp. 1-6, Oct. 2019.

C2. **J. Yuan**, Y. Yang, P. Liu, and F. Blaabjerg, "An Embedded Switched-Capacitor Z-Source Inverter with Continuous Input Currents" in *Proc. IEEE APEC*, pp. 2366-2371, May 2019.

C3. **J. Yuan**, Z. Shen, Y. Yang, A. Mostaan and F. Blaabjerg, "Design and Analysis of a Novel Trans-inverse DC-DC Converter" in *Proc. IEEE COMPEL*, pp. 1-5, Jul. 2019.

C4. **J. Yuan**, Y. Yang, and F. Blaabjerg, "Systematic Design of Impedance Source Inverters" in *Proc. IEEE COMPEL*, 2020, under review.

The publications done during the study but are not included in the Ph.D. thesis are listed below:

- **J. Yuan**, Y. Chen, Y. Yang, F. Blaabjerg and M. Chen, "High Frequency Multicell Cascaded Quasi-Square-Wave Boost Converter" in *Proc. IEEE COMPEL*, 2020, under review.

  J. Yuan, Y. Yang, and F. Blaabjerg, "Leakage Current Mitigation in Transformerless Z-Source/Quasi-Z-Source PV Inverters: An Overview" in *Proc. IEEE ECCE*, pp. 2603-2608, Nov. 2019.
- **J. Yuan**, Y. Yang, P. Liu and F. Blaabjerg, "Model Predictive Control of An Embedded Enhanced-Boost Z-Source Inverter" in *Proc. IEEE COMPEL*, pp. 1-6, Sep. 2018.
- P. Wang, Y. Chen, **J. Yuan**, R. C. N. Pilawa-Podgurski and M. Chen, "Hardware, Software, and Power Co-Design of a Data Storage Server with Differential Power Processing", *IEEE Trans. Power Electron.*, under review.
- P. Liu, Y. Yang, **J. Yuan**, and F. Blaabjerg, "Model Predictive Control for Quasi-Z Source Inverters with Improved Thermal Performance" in *Proc. IEEE COMPEL*, pp. 2603-2608, Sep. 2018.
- P. Liu, Y. Yang, C. Tu, **J. Yuan** and F. Blaabjerg,"A Novel PWM Strategy for Current Ripple and Output Harmonic Minimization of Current-Fed Trans-Quasi-Z-Source Inverters," in *Proc. IEEE IECON*, pp. 3700-3705, Nov. 2018.
- W. Liu, **J. Yuan**, Y. Yang and T. Kerekes, "Modeling and Control of Single-Phase Quasi-Z-Source Inverters," in *Proc. IEEE IECON*, pp. 3737-3742, Nov. 2019.

Chapter 2

2 Improved Impedance-Source Inverters

To address the limitations of the existing ZSIs, three improved ZSIs are proposed as the effective single-stage DC-AC solutions in this thesis. This chapter presents three improved ZSI topologies and their operational principles. The improved topologies are based on the switched-inductor, switched-capacitor and the active switch, which will be discussed in terms of continuous input current, high voltage gain, low voltage stresses across the components, and fault-tolerant operations. In addition, some benchmarking of various ZSIs are summarized to show the superior performance of improved ZSIs.

2.1 Modified Embedded Z-Source Inverters

As discussed in *Chapter 1*, the embedded structure can allow the continuous input current, and its multisource structure makes it attractive for renewable energy applications (e.g., PV application). However, the boosting capability of the basic embedded-ZSI is very limited. Therefore, two modified enhanced-boost embedded-ZSI are introduced in this thesis. As observed in Fig. 2.1 and Fig. 2.2, an embedded enhanced-boost ZSI (EEB-ZSI) [J1], [21] and an embedded switched-capacitor ZSI (ESC-ZSI) [C3], [25] are proposed by rearranging the position of the components and dc sources, where two DC sources are adopted and symmetrically inserted throughout the impedance network based on the topologies proposed in [73, 74]. Moreover, compared to similar prior-art topologies [51–60], these two topologies not only have the characteristics of the embedded structure but also inherit the advantages of enhanced-boost ZSI in terms of high boosting ratios. The characteristics of the EEB-ZSI and ESC-ZSI are similar, hence, the theoretical analysis is only performed based on the EEB-ZSI in the following section.

2.1.1 Operation Principle Analysis

As presented in Fig. 2.1, the EEB-ZSI incorporates two symmetrical impedance networks, where one network is made up of C_1, C_2, L_1, and L_2, and the other one consists of C_3, C_4, L_3, and L_4 [J1], [21]. The inductor currents are specified as i_{L1}, i_{L2}, i_{L3}, and i_{L4} [J1], [21]. The capacitor voltages are expressed as V_{C1}, V_{C2}, V_{C3}, and V_{C4} [J1], [21]. The current of the phase-a is i_a [J1], [21]. Similar to conventional ZSIs,

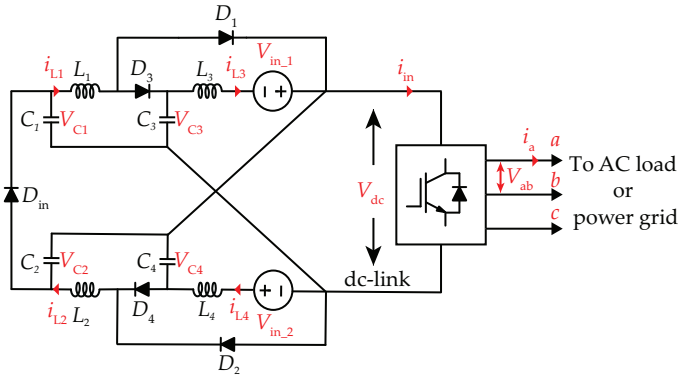


Fig. 2.1: Schematic of the embedded enhanced-boost Z-source inverter (EEB-ZSI) [J1], [21].

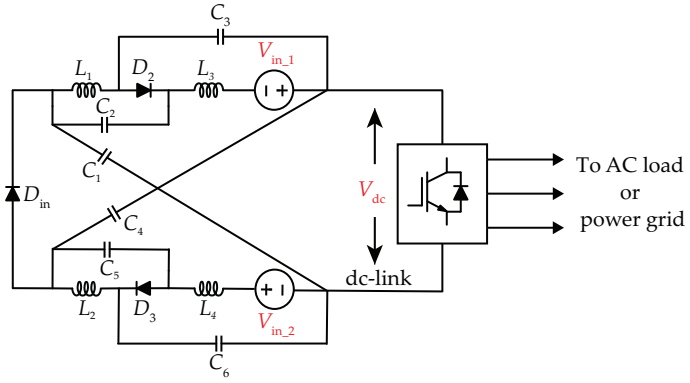


Fig. 2.2: Schematic of the embedded switched-capacitor Z-source inverter (ESC-ZSI) [C3], [25].

there are two operation states (e.g., ST and NST states) in the EEB-ZSI [J1], [21]. The equivalent circuits of the EEB-ZSI are presented in Fig. 2.3.

In Fig. 2.3(a), the dc-link side is short-circuited when the switches on one inverter bridge turn on at the same time during the ST state, where D_1 and D_2 are in the ON-state because they are forward-biased. In comparison, D_3 and D_4 are reverse-biased. In addition, D_{in} is also reverse-biased. In the mean time, the capacitors C_1-C_4 are charging the inductors L_1-L_4, as it is indicated in Fig. 2.3(a).

During the NST state in Fig. 2.3(b), D_1 and D_2 are reverse-biased and D_3, D_4 and D_{in} are ON-state. Compared with the ST state, the capacitors are charged by the DC sources while the load/grid side receives the stored energies from the inductors [J1], [21].

As indicated in Fig. 2.3, the basic relationship among variables can be derived. Furthermore, through several derivations as reported in [J1], [21], the peak dc-link

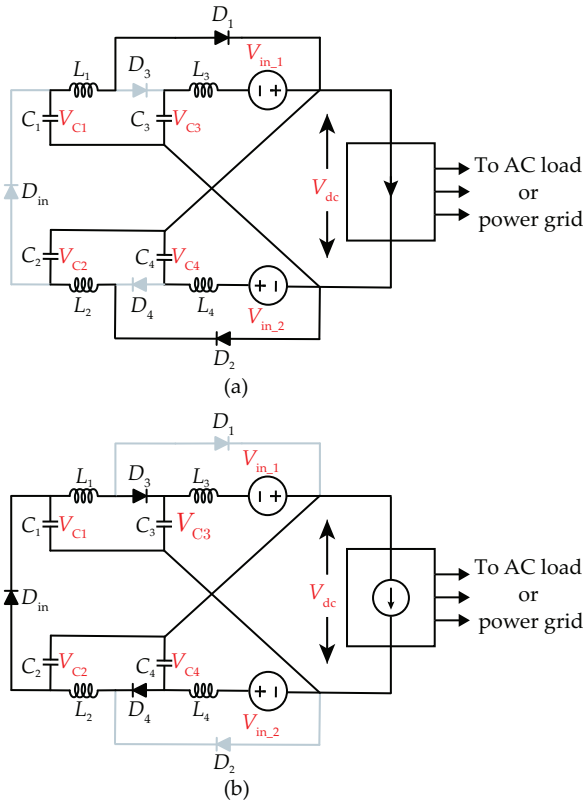


Fig. 2.3: The operation topologies of the embedded enhanced-boost Z-source inverter: (a) equivalent circuit during the shoot-through state, and (b) equivalent circuit during the non-shoot-through state [J1], [21].

voltage $V_{\mathrm{dc}}^{\mathrm{p}}$ is expressed as

$$V_{\mathrm{dc}}^{\mathrm{p}} = \frac{1-D}{2D^2-4D+1}(V_{\mathrm{in\_1}} + V_{\mathrm{in\_2}}) = B \cdot (V_{\mathrm{in\_1}} + V_{\mathrm{in\_2}}) \tag{2.1}$$

where

$$B = \frac{1-D}{2D^2-4D+1} \tag{2.2}$$

is the boost factor, D is the duty cycle, and $V_{\mathrm{in\_1}}$ and $V_{\mathrm{in\_2}}$ represent the input voltages. Additionally, the peak of the inverter output voltage is derived as

$$V_{\mathrm{ac}}^{p} = \frac{MV_{\mathrm{dc}}^{p}}{2} = \frac{MBV_{\mathrm{dc}}}{2} = \frac{GV_{\mathrm{dc}}}{2} \tag{2.3}$$

where G is the voltage gain, M is the modulation index, and V_{dc} is the average dc-link voltage [J1], [21]. Furthermore, the voltage gain is expressed as

$$G = MB = \frac{M^2}{2M^2-1}. \tag{2.4}$$

It is worth to note that in a certain range of the duty cycles, the boost factors are infinite according to Eq. (2.2). However, it is impractical considering parasitic parameters of the components as well as available devices. In addition, according to the basics of modulation methods, the sum of D and M should not be larger than one. Therefore, a larger G is achieved with a lower M, which results in low power quality and higher power losses [J1], [21].

2.1.2 Fault-Tolerant Operations

The fault-tolerant capabilities of power converters are critical to the reliability of renewable energy systems [J1], [21]. It should be noted that the previous studies about ISN topologies with fault-tolerant capabilities concentrate primarily on the switch failure [75, 76]. In addition to switch faults, however, the faulty input sources may trigger serious consequences, e.g., system shutdown and economic losses. For example, the shading phenomenon can bring about different currents if multi-PV-panels are employed [77]. Even for the one-source system, the faults, such as open-circuit or short-circuit, may occur. Nevertheless, in such cases, prior-art topologies cannot achieve the fault-tolerant operation under faulty conditions. Hence, novel ISNs with fault-tolerant capabilities, high boosting capabilities and continuous input current, need to be explored for PV applications [77]. Accordingly, the EEB-ZSI features fault-tolerant capability under abnormal conditions of the dc sources, i.e., open-circuit (OC), short-circuit (SC) and unbalance [J1], [21].

- Open-circuit Analysis
  As indicated in Fig. 2.4, the EEB-ZSI operates when one dc source is open-circuited. The corresponding circuit diagram of the EEB-ZSI is shown in Fig. 2.4(a). It is noticeable in Fig. 2.4(b) and (c) that there is no power transmission regarding the C_4 and L_4. Compared with the previous analysis of the operation modes, D_2 is always in the conduction mode and D_4 is reverse-biased during the ST and NST states. Similarly, $V_{\mathrm{dc}}^{\mathrm{p}}$ and G are expressed as

$$V_{\mathrm{dc}}^{\mathrm{p}} = \frac{1-D}{D^2-3D+1} \cdot V_{\mathrm{in\_1}} \tag{2.5}$$

$$G = M \cdot B = \frac{M^2}{M^2+M-1}. \tag{2.6}$$

  By comparing Eqs. (2.2), (2.4) with (2.5), (2.6), it is clear that B and G with one dc source being open-circuited are lower in contrast to normal mode. Nevertheless, the reduced boosting capability due to the OC fault can be compensated by adjusting the D and M.

- Short-circuit Analysis
  When an SC fault occurs in the EEB-ZSI, normal operation of the EEB-ZSI can still be ensured. Fig. 2.5 present the equivalent circuits under SC faulty mode. Although the SC fault happens in the EEB-ZSI, the operation in this case remains the same. Nonetheless, the input power from the dc source is only half of the original power in the normal condition. Similarly, $V_{\mathrm{dc}}^{\mathrm{p}}$ and G can be derived as

$$V_{\mathrm{dc}}^{\mathrm{p}} = \frac{1-D}{2D^2-4D+1} \cdot V_{\mathrm{in\_1}} \tag{2.7}$$

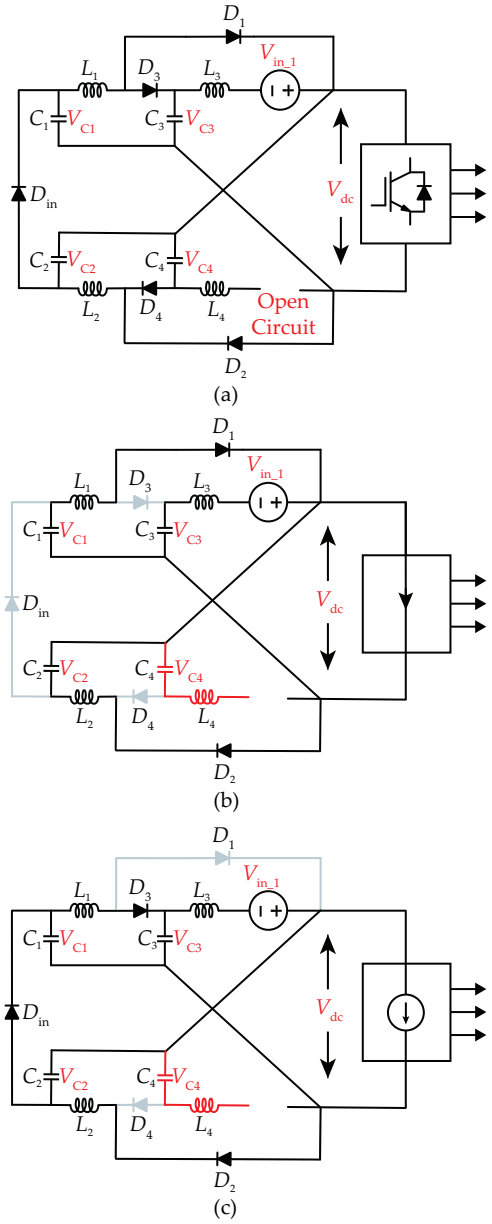


Fig. 2.4: Proposed EEB-ZSI with one source being open-circuited: (a) system schematic, (b) operation mode during the ST state, and (c) operation mode during the NST state [J1], [21].

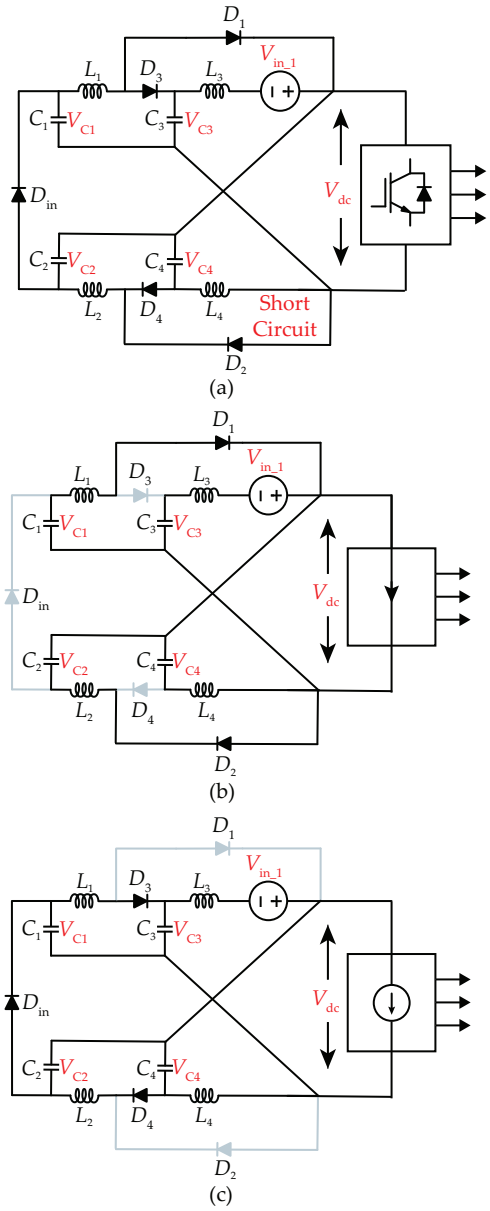


Fig. 2.5: Proposed EEB-ZSI with one source being short-circuited: (a) system schematic, (b) operation mode during the ST state, and (c) operation mode during the NST state [J1], [21].

Table 2.1: Benchmarking of Boosting Capability the EEB-ZSI under Normal and Faulty Condition [J1], [21]

	Normal Operation	Open-circuit	Short-circuit
Boost factor, B	$\frac{1-D}{2D^2-4D+1}$	$\frac{1-D}{D^2-3D+1} \cdot \frac{1}{2}$	$\frac{1-D}{2D^2-4D+1} \cdot \frac{1}{2}$
Voltage gain, G	$G = \frac{M^2}{2M^2-1}$	$G = \frac{M^2}{M^2+M-1}$	$G = \frac{M^2}{4M^2-2}$

$$G = M \cdot B = \frac{M^2}{4M^2 - 2}. \tag{2.8}$$

According to the above equations, G under SC condition is only half of the normal operation. Table 2.1 presents the comparison in regards to boost factor and voltage gain under normal and abnormal conditions, and Fig. 2.6 shows their relationship. As observed in Fig. 2.6, the expected G could be guaranteed by changing the D and M. That is, the fault-tolerant capability can be obtained by selecting D and M under abnormal conditions.

- Source-Unbalance Analysis

  It should be noted that in PV systems, the voltage of the PV panels may be different, considering the PV panels operate under a partially shaded condition. In fact, the input currents from the PV panels should be identical if the same panels are adopted. For convenience, the input voltage can be defined as V_1 and V_2. Obviously, the operation principle is not affected in this condition. Therefore, according to above-mentioned analysis, the $V_{\mathrm{dc}}^{\mathrm{p}}$ is expressed as

$$V_{\mathrm{dc}}^{\mathrm{p}} = \frac{1 - D}{2D^2 - 4D + 1} \cdot (V_{\mathrm{in\_1}} + V_{\mathrm{in\_2}}). \tag{2.9}$$

  Compared with Eq. (2.2), they have the same expression of the boost factor. However, $V_{\mathrm{dc}}^{\mathrm{p}}$ may fluctuate under the SC condition. It is noted that by comparing the Eqs. (2.7) and (2.9), the SC condition is considered as the special unbalance case.

2.1.3 Comparison Analysis

To perform a comprehensive comparison regarding the boosting capability and voltage stresses, the selected topologies, the basic ZSI [18], embedded-ZSI (E-ZSI) [51], diode-assisted ZSI (DA-ZSI) [37], switched-inductor ZSI (SI-ZSI) [27], enhanced-boost ZSI (EB-ZSI) [78], are utilized to compare with the EEB-ZSI [J1], [21]. In Fig. 2.7(a), it is clear that the boost factor of the EEB-ZSI is slightly smaller than that of the EB-ZSI, but it is larger than the other selected ZSIs due to the extra inductors (L_1-L_4) [J1], [21]. Furthermore, the comparison results between the prior-art topologies and the EEB-ZSI by considering the voltage gain and modulation index is presented in Fig. 2.7(b). It is straightforward in Fig. 2.7(b) that the EEB-ZSI has larger voltage gains than most of the selected topologies under a wide range of M. It is recognized that power quality is mainly determined by the modulation index. Therefore, according to Fig. 2.7(b), higher modulation index could be applied in the EEB-ZSI and EB-ZSI for the same boosting capability in contrast to other selected topologies.

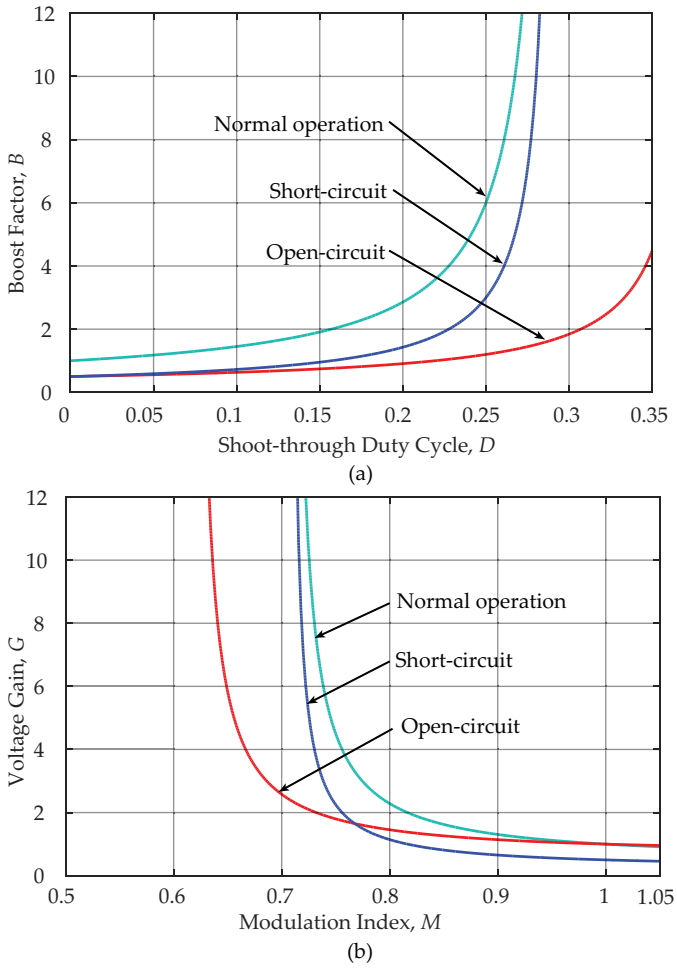


Fig. 2.6: Comparison of the EEB-ZSI under normal and faulty conditions: (a) boost factor versus duty cycle, and (b) voltage gain versus modulation index [J1], [21].

Aside from the superior performance regarding the boosting capability, the EEB-ZSI can benefit from low voltage stresses across the components [J1], [21]. To simplify the comparison process, the voltage stresses are expressed as the proportion of the peak dc-link voltage and voltages of switches and capacitors to GV_{in} [21, 79]. It is evident in Fig. 2.8(a) that lower rating power switches could be applied in the EEB-ZSI compared to other topologies. Additionally, although the EEB-ZSI and EB-ZSI have the same component count, the EEB-ZSI has the better performance in terms of voltage stresses across the capacitors, as shown in Fig. 2.8(b). Therefore, the EEB-ZSI may apply the capacitor with lower ratings to reduce the cost and size.

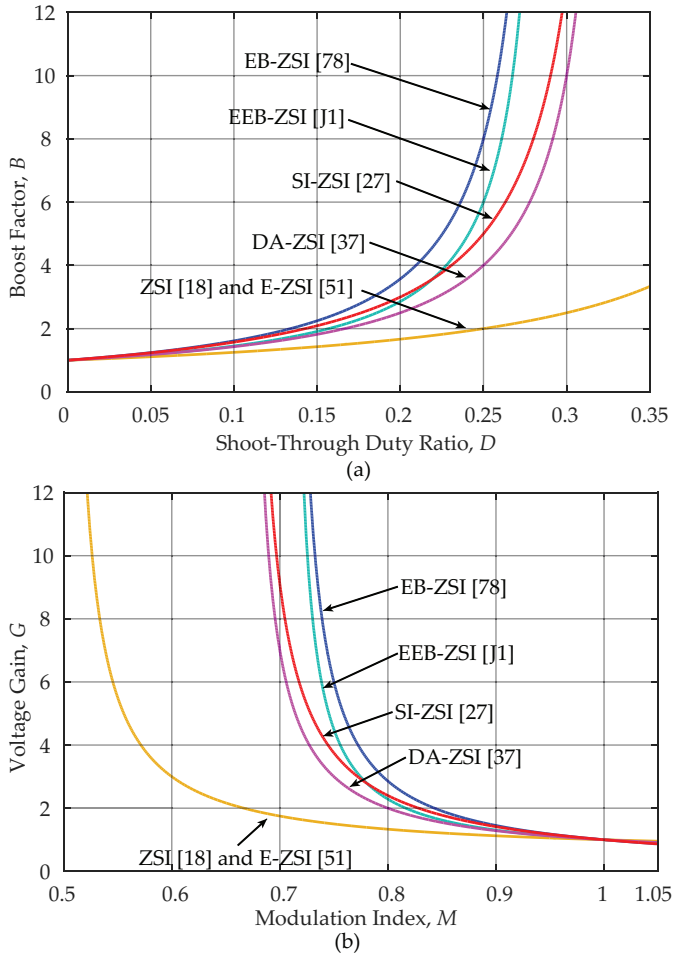


Fig. 2.7: Comparison of the prior-art topologies with the EEB-ZSI: (a) B versus D, and (b) G versus M [J1], [21].

2.1.4 Experimental Verification

To verify the steady-state operation and fault-tolerance performance of the EEB-ZSI, experimental results are provided in this section. The normal operation case and faulty cases (i.e., OC, SC and unbalance source modes) are conducted to validate the theoretical analysis. M and D are set as 0.85 and 0.15, respectively, in the initial state [J1], [21]. Table 2.2 shows the key parameters of the experimental tests.

Case 1. Fig. 2.9 presents the experimental results when the EEB-ZSI works in the normal condition. In this case, the peak dc-link voltage and inverter output voltage are boosted from 80 V to 150 V [J1], [21]. Compared to the theoretical value, the boosted voltage is marginally lower due to the parasitics of the components. Additionally, the inductor current i_{L3} remains continuous. As for the load current i_a, its peak value is around 1.8 A, as shown in Fig. 2.9.

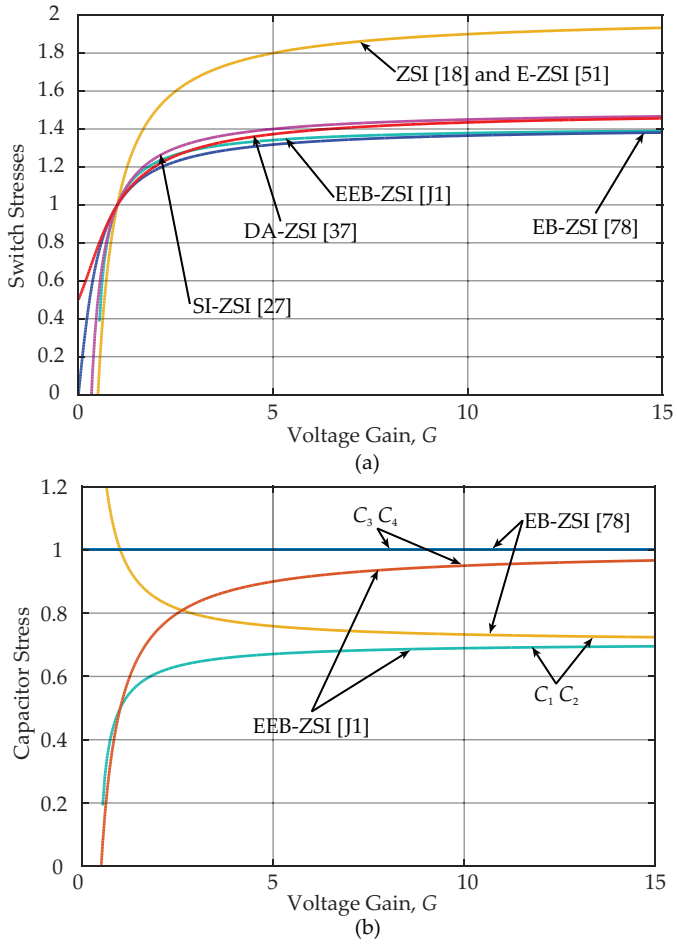


Fig. 2.8: Comparison of the prior-art topologies with the EEB-ZSI: (a) normalized voltage stress on the power switches, and (b) normalized capacitor voltage stress of the EB-ZSI and the EEB-ZSI [J1], [21].

Case 2. The experimental results with an OC fault are indicated in Fig. 2.10. It is clear in Fig. 2.10 that from 0 to 0.1 s, the output voltage could be boosted to 60 V in the initial state with M and D being 0.85 and 0.15, respectively. The obtained results are consistent with the previous analysis, according to Eq. (2.5). Furthermore, to achieve the fault-tolerant operation under the OC condition, the modulation index and duty cycle should be configured to 1 and 0.305, respectively, at 0.1 s based on the previous analysis. Fig. 2.10 shows the dc-link and output voltages have reached expected values, which are similar to the results in Fig. 2.9. In addition, the increased inductor current (i_{L3}) implies that more power is being transmitted and the load current is also increasing relative to the initial state.

Table 2.2: Specifications for the EEB-ZSI [J1], [21]

Parameter	Symbol	Value
DC input voltage	V_{in}	80 V
Power Rating	P	500 W
EEB-ZSI inductance	L_1, L_2, L_3, L_4	640 μH
EEB-ZSI capacitor	C_1, C_2, C_3, C_4	100 μF
Load inductance	L_f	6 mH
Load resistance	R_f	40 Ω
Switching frequency	f_s	5 kHz

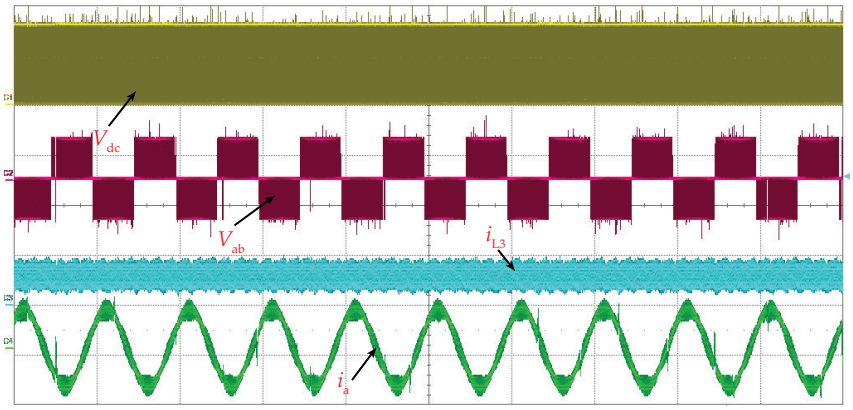


Fig. 2.9: Experimental results of the EEB-ZSI under normal operation: V_{dc} [100 V/div], V_{ab} [200 V/div], i_{L3} [5 A/div], i_a [2 A/div], time [20 ms/div] [J1], [21].

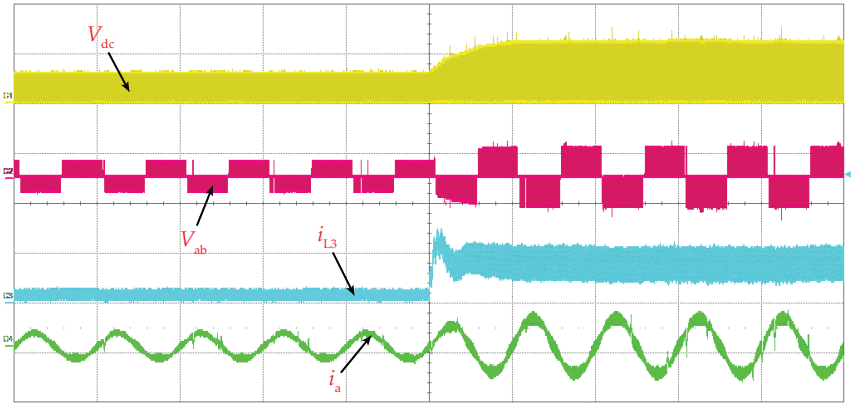


Fig. 2.10: Experimental results of the EEB-ZSI under open-circuit operation: V_{dc}[100 V/div], V_{ab}[200 V/div], i_{L3}[5 A/div], i_a [2 A/div], time [20 ms/div] [J1], [21].

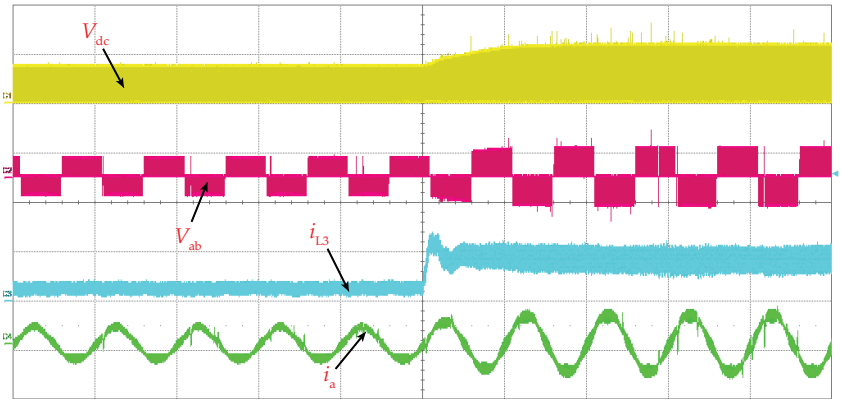


Fig. 2.11: Experimental results of the EEB-ZSI under short-circuit operation: V_{dc} [100 V/div], V_{ab} [200 V/div], i_{L3} [5 A/div], i_a [2 A/div], time [20 ms/div] [J1], [21].

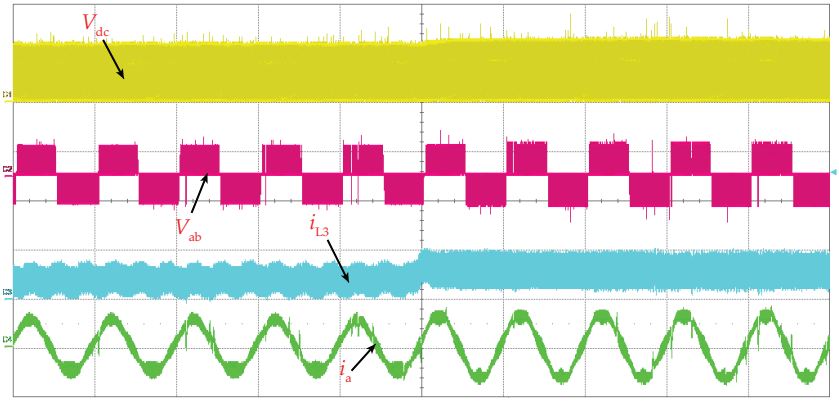


Fig. 2.12: Experimental results of the EEB-ZSI under unbalanced source operation: V_{dc} [100 V/div], V_{ab} [200 V/div], i_{L3} [5 A/div], i_a [2 A/div], time [20 ms/div] [J1], [21].

Case 3. The last case is conducted with the two sources being unbalanced. Compared with the normal operation, the operation principle in the SC case is similar. Nonetheless, the peak dc-link voltage is around 76 V from the beginning, which validates only half boosting capability is achieved under unbalanced condition, as shown in Fig. 2.11. In the same way, the required voltage could be ensured by regulating M and D to 1 and 0.219, respectively. Additionally, the unbalanced condition is shown in Fig. 2.12. The power sources provide 40 V and 20 V, respectively. It can be indicated in Fig. 2.12 that the dc-link voltage is 114 V, which is the same as the theoretical analysis in Eq. (2.9). Similarly, adjusting M and D can ensure the boosted voltage to be the normal level, as shown in Fig. 2.12.

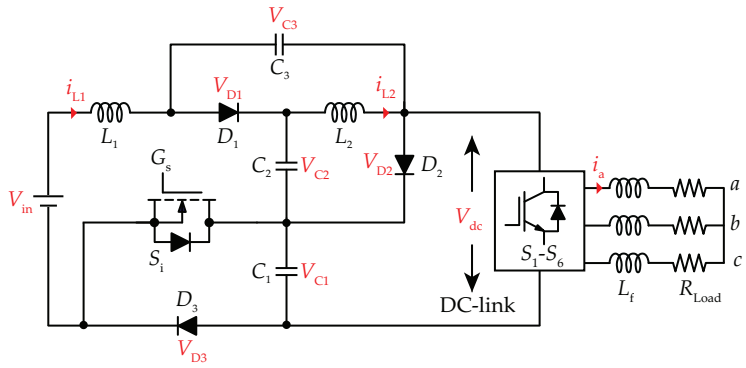


Fig. 2.13: Circuit topology of the proposed switched-quasi-Z-source inverter (S-qZSI) [J2], [80].

2.2 Switched Quasi-Z-Source Inverter

As discussed previously, the switched ZSIs are important topologies, which can achieve a high boosting ratio with fewer components compared with other ZSI/qZSIs. In this section, a switched boost network-based qZSI (S-qZSI) is introduced [J2], [80]. It features a continuous input current and improved boosting ratios compared with its counterparts. The operation principles are demonstrated extensively. In addition, a benchmarking in regard to the conversion ratios as well as voltage stresses over the components is conducted between prior-art ZSIs and the proposed S-qZSI.

Fig. 2.13 indicates the circuit topology of the S-qZSI. As indicated in Fig. 2.13, there are two inductor (L_1 and L_2), three capacitors (C_1, C_2, and C_3), three diodes (D_1, D_2, and D_3), and one active switch (S_i) in the main topology [J2], [80]. Moreover, a resistive-inductive load is implemented to the main topology by a conventional VSI. The voltages across the capacitors are defined as V_{C1}, V_{C2}, and V_{C3}, and the diode voltages are denoted as V_{D1}, V_{D2}, V_{D3} [J2], [80]. i_{L1} and i_{L2} represent the currents through the inductors L_1 and L_2, and i_a is the load current [J2], [80].

2.2.1 Operation Principle of the S-qZSI

The operation principle of the S-qZSI is just like other impedance-source inverters, so the equivalent circuits during the ST and NST states are indicated in Fig. 2.14. Moreover, the steady-state analysis is presented in Fig. 2.15.

During the ST states in Fig. 2.14(a), the switch S_i is turned ON and the dc-link side is short-circuited. From Fig. 2.15, the diode voltages are all negative, i.e., reverse-biased. At the same time, the inductors are charged by the input source and capacitors. Fig. 2.15 shows that the inductor currents have a ascending tendency from t_1 to t_2 during the ST state. On the contrary, the switch S_i is turned ON and the S-qZSI operates like a traditional VSI. Additionally, three diodes are in the OFF-state and the diode voltages are zero in Fig. 2.15. Meanwhile, the energy stored in the inductors is transferred to the load side during the NST state, and the voltage is boosted as expected. According to the Kirchhoff's law and volt-second balance principle, the

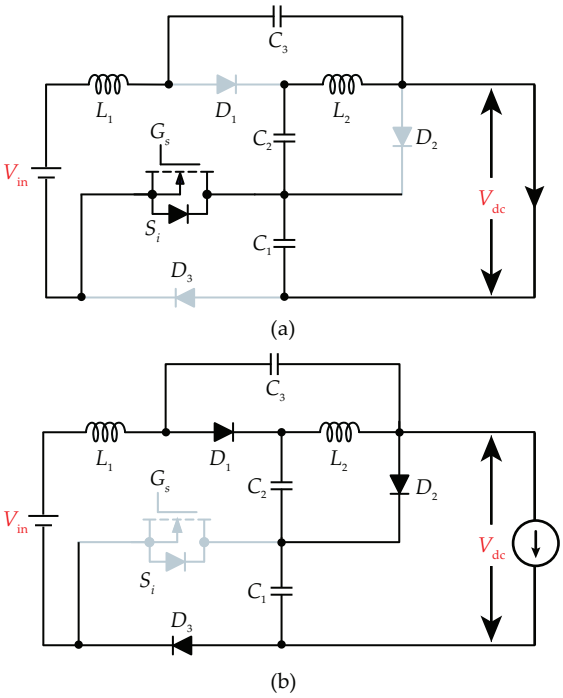


Fig. 2.14: Operation modes of the S-qZSI: (a) shoot-through state, and (b) non-shoot-through state [J2], [80].

boost factor B and voltage gain G are expressed as [J2], [80]

$$B = \frac{1}{1-3D} \tag{2.10}$$

$$G = MB = \frac{M}{3M-2}. \tag{2.11}$$

2.2.2 Comparison Analysis

A comparative analysis among switched boost inverter (SBI) [38], embedded-qSBI [39], Diode-assisted SBI (DA-SBI) [42], continuous input current qZSI (CC-qZSI) [44], and the S-qZSI, in terms of component count, boosting capability, and component stresses is carried out.

At first, Table 2.3 shows the component counts of the S-qZSI and other selected topologies. According to Table 2.3, two inductors are utilized in the S-qZSI, DA-SBI and CC-qZSI, however, only one inductor is used in the original SBI and embedded-qSBI. Additionally, by comparing the S-qZSI and DA-ZSI, they have the same components and the S-qZSI utilizes one more capacitor instead of a diode to obtain the qZS network.

Additionally, Table 2.4 summarizes the benchmarking results regarding the B, G, and component stress between the S-qZSI and prior-art topologies [J2], [80]. The

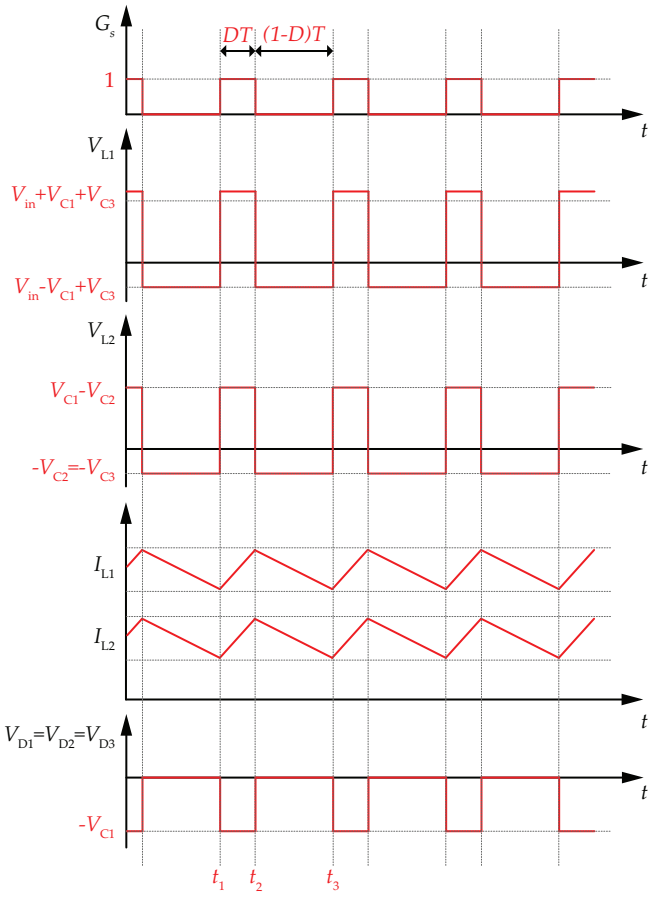


Fig. 2.15: Operation waveform of the S-qZSI [J2], [80].

comparative study of the boosting capability is shown in Fig. 2.16. In Fig. 2.16(a), the S-qZSI may achieve the highest boosting ratio under certain duty cycle ranges (i.e., 0-0.3) compared with other topologies. Especially, its boosting capability is greatly improved without adding more components compared to the DA-SBI. From another point of view, Fig. 2.16(b) shows that a higher M can be utilized with the same G in the S-qZSI relative to other topologies. Hence, a higher M can make the power quality better to a certain extent.

In addition to the good performance of boosting capability, as discussed above, voltage stresses of the S-qZSI across the components are relatively low among all the selected topologies. The expressions for the power switch, the capacitors and the diodes on the main topology, and switches on inverter bridges are listed in Table 2.4. Moreover, the comparison of voltage stresses for the components are shown in Fig. 2.17 and Fig. 2.18.

To give a fair comparison, the voltage stress could be denoted as the expression that voltage across the components divided by GV_{in}. In Fig. 2.17(a), the voltage stress across

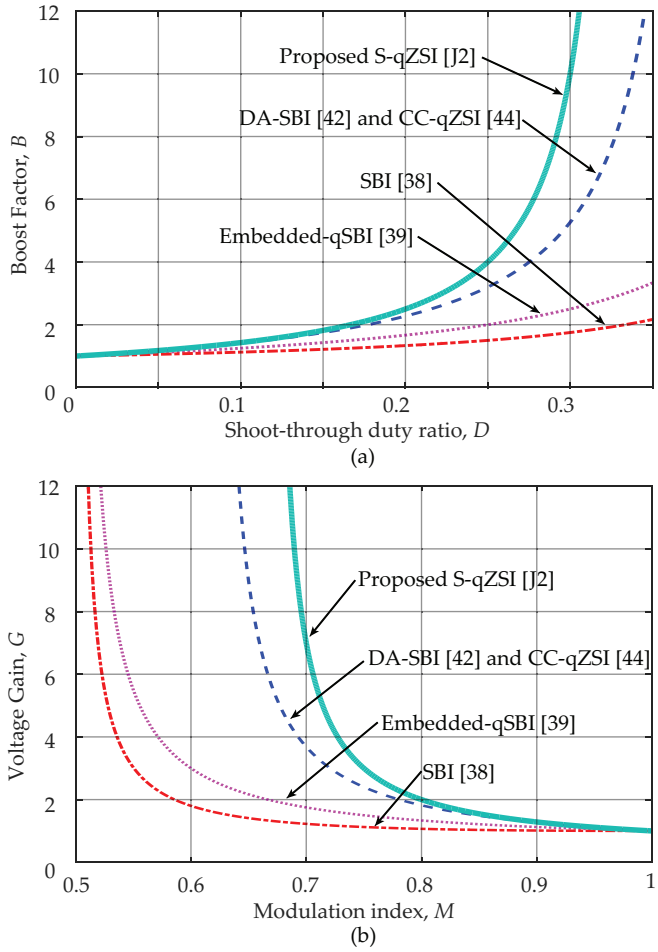


Fig. 2.16: Comparison of the prior-art topologies with the EEB-ZSI: (a) boost factor B versus the shoot-through duty-ratio D, and (b) voltage gain G versus the modulation index M [J2], [80].

the network-switch of the SBI and DA-SBI is higher than that of the S-qZSI despite having the same components. In terms of the stress of inverter bridge switches (S_1-S_6), the S-qZSI also shows the best performance compared with other topologies, where lower rating components may be utilized to optimize the cost. As for the capacitor stress in Fig. 2.18(a), the S-qZSI has lower capacitor stresses than other topologies except for the CC-qZSI. Likewise, in comparison to other selected topologies (excluding the embedded-qSBI), the voltage stresses over the didoes of the S-qZSI is much lower.

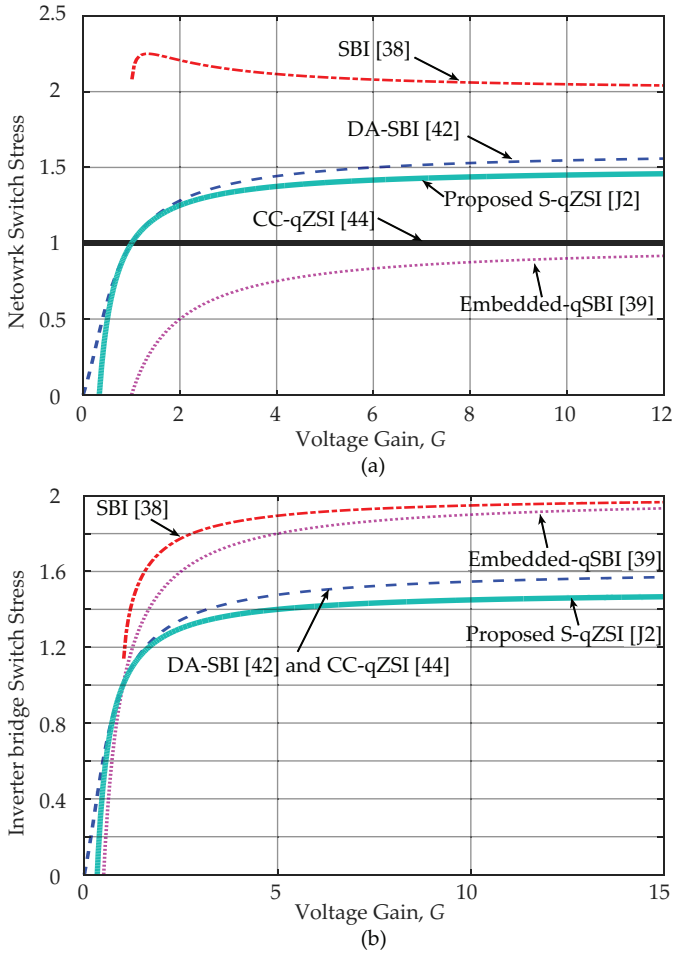


Fig. 2.17: Voltage stress comparison of the prior-art topologies with the EEB-ZSI: (a) voltage stress on the network switch, and (b) voltage stress on the inverter bridge [J2], [80].

2.2.3 Experimental Verification

To validate the operation principle and characteristics of the S-qZSI concerning continuous input currents and low voltage stress, the prototype of the E-qZSI is built up and the key parameters of the S-qZSI are listed in Table 2.5 [J2], [80]. Furthermore, the complementary signals are generated by the use of Texas Instruments TMS320F28335 digital signal processor (DSP) and further logical operation for the output signals can be performed on the field-programmable gate array (FPGA) from Altera company.

The experimental results in Fig. 2.19 are obtained by setting M = 0.83 and D = 0.25. According to Eq. (2.10), the DC-link voltage is increased to 120 V with D being 0.25. As observed in Fig. 2.19(a), the peak V_{dc} is around 116 V and i_a is about 1.8 A, respectively. Therefore, compared to the theoretical value, it is clear that the boosting

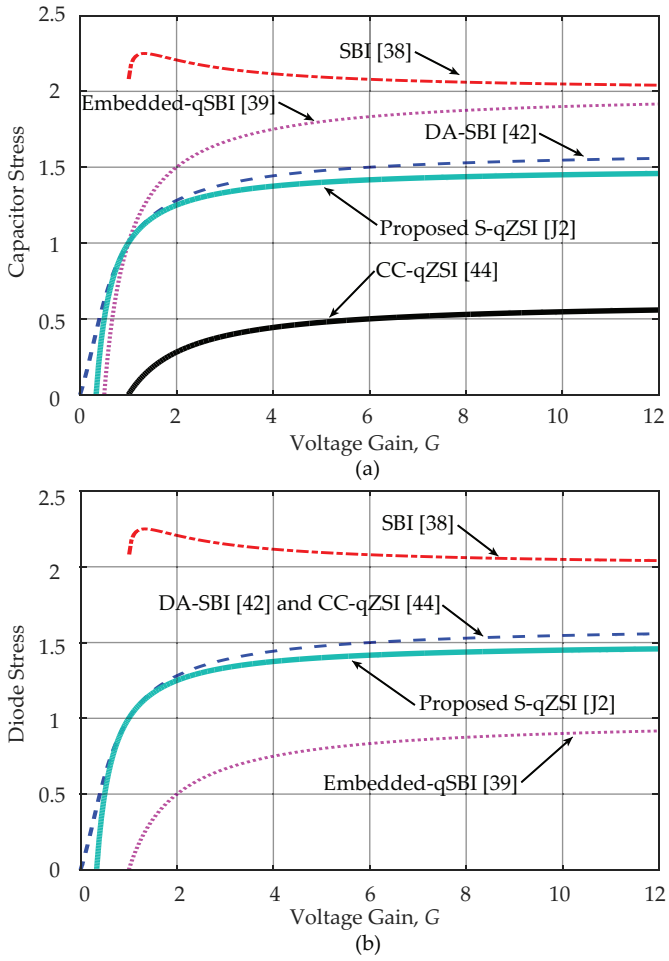


Fig. 2.18: Voltage stress comparison of the prior-art topologies with the EEB-ZSI: (a) voltage stress on the capacitor (C_1), and (b) voltage stress on the diode (D_1) [J2], [80].

capability in the experimental test is slightly reduced, which can be explained by that the performance of the S-qZSI is affected by the parasitic from the components and printed circuit board (PCB). As for inductor currents presented in Fig. 2.19(b), the inductor currents increase linearly to store the energy during the ST state. In constrast, the voltage-boosting can be achieved by delivering the energy from inductor to the load during the NST state. Moreover, the inductor current i_{L1} shows that the input current maintains a continuous state. In Fig. 2.19(c), the gate signal and diode voltages are presented, where the diode voltages have the same values and their peak values are equal to V_{dc}. At last, Fig. 2.19(d) presents the capacitor voltages. The capacitor voltage V_{C1} is about 116 V, which is consistent with V_{dc}. Meanwhile, the voltages across C_2 and C_3 are identical to V_{in} (e.g., 30 V).

Table 2.3: Benchmarking of the Component Count among Prior-Art Topologies and the Proposed S-qZSI [J2], [80]

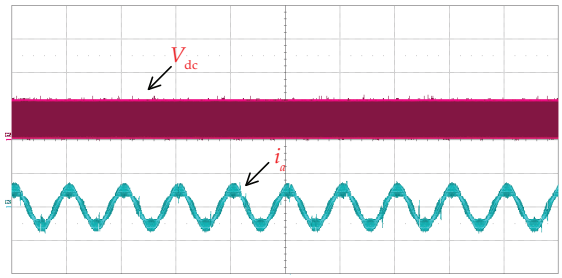
Component	SBI [38]	Embedded-qSBI [39]	DA-SBI [42]	CC-qZSI [44]	S-qZSI
Inductors	1	1	2	2	2
Capacitors	1	1	2	2	3
Switches	1	1	1	1	1
Diodes	2	2	4	2	3

Table 2.4: Benchmarking of Boost Factor, Voltage Gain, and Voltage Stresses among Prior-Art Topologies and the Proposed S-qZSI [J2], [80]

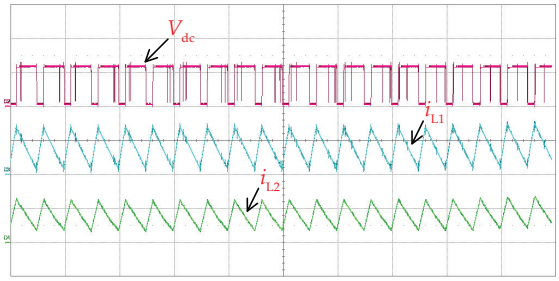
	SBI [38]	Embedded-qSBI [39]	DA-SBI [42]	CC-qZSI [44]	S-qZSI
B	$\frac{1-D}{1-2D}$	$\frac{1}{1-2D}$	$\frac{1}{D^2-3D+1}$	$\frac{1}{D^2-3D+1}$	$\frac{1}{1-3D}$
G	$\frac{M^2}{2M-1}$	$\frac{M}{2M-1}$	$\frac{M}{M^2+M-1}$	$\frac{M}{M^2+M-1}$	$\frac{M}{3M-2}$
$\frac{V_{S_i}}{GV_{in}}$	$\frac{1}{G-\sqrt{G^2-G}}+\frac{1}{G}$	$1-\frac{1}{G}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	1	$\frac{3G-1}{2G}$
$\frac{V_{S_1}}{GV_{in}}$	$\frac{1}{G-\sqrt{G^2-G}}$	$2-\frac{1}{G}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	$\frac{3G-1}{2G}$
$\frac{V_{C_1}}{GV_{in}}$	$\frac{1}{G-\sqrt{G^2-G}}$	$2-\frac{1}{G}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}-1$	$\frac{3G-1}{2G}$
$\frac{V_{C_2}}{GV_{in}}$	/	/	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}-1$	1	$\frac{G-1}{2G}$
$\frac{V_{C_3}}{GV_{in}}$	/	/	/	/	$\frac{G-1}{2G}$
$\frac{V_{D_1}}{GV_{in}}$	$\frac{1}{G-\sqrt{G^2-G}}+\frac{1}{G}$	$1-\frac{1}{G}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	$\frac{3G-1}{2G}$
$\frac{V_{D_2}}{GV_{in}}$	$\frac{1}{G-\sqrt{G^2-G}}$	$2-\frac{1}{G}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	1	$\frac{3G-1}{2G}$
$\frac{V_{D_3}}{GV_{in}}$	/	/	1	/	$\frac{3G-1}{2G}$
$\frac{V_{D_4}}{GV_{in}}$	/	/	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}-1$	/	/

Table 2.5: System specifications of the proposed S-qZSI [J2], [80]

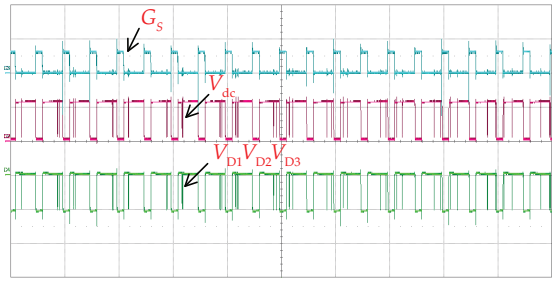
Parameter	Symbol	Value
Modulation index	M	0.83
Duty cycle	D	0.25
DC input voltage	V_{in}	30 V
Power rating	P	250 W
S-qZSI inductance	L_1, L_2	643 μH
S-qZSI capacitor	C_1, C_2, C_3	100 μF
Load inductance	L_f	3 mH
Load resistance	R_f	40 Ω
Switching frequency	f_s	5 kHz



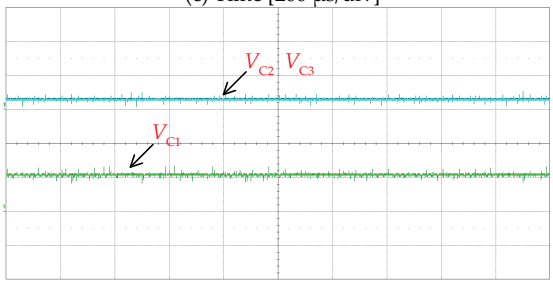
(a) Time [20 ms/div]



(b) Time [200 µs/div]



(c) Time [200 µs/div]



(d) Time [1 ms/div]

Fig. 2.19: Experimental results of the S-qZSI: (a) DC-link voltage V_{dc} [100 V/div] and output phase-a current i_a [2 A/div], (b) DC-link voltage V_{dc} [100 V/div] and inductor currents i_{L1}, i_{L2} [5 A/div], (c) gate signal G_s [20 V/div], DC-link voltage V_{dc} [100 V/div] and diode voltage V_{D1}, V_{D2}, V_{D3} [100 V/div], and (d) capacitor voltage V_{C1}, V_{C2}, V_{C3} [100 V/div] [J2], [80].

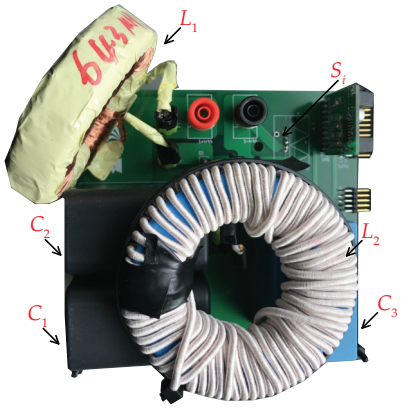


Fig. 2.20: Photograph of the 250 W prototype of the switched-impedance source network [J2], [80].

2.3 Summary

This chapter introduces two improved ZSIs: the EEB-ZSI and the S-qZSI. For the EEB-ZSI, the operation principles and a comparative study in terms of boosting capability and voltage stress are discussed. Furthermore, the fault-tolerant operations of the EEB-ZSI are studied under abnormal conditions. The effectiveness of the EEB-ZSI is validated through experimental tests. In addition, the new S-qZSI is discussed. The S-qZSI features improved boosting capability, continuous input current as well as low voltage stresses, which has been validated by the benchmarking and experimental tests.

Chapter 3

3 Modified Impedance-Source DC-DC Converters

In addition to applying ISNs to the single-stage power conversion systems, ISNs also could be applied as first-stage DC-DC converters as two-stage solutions. Compared to the basic boost converter, the boost converters with ISNs feature improved conversion ratios and low voltage stress across the components. As discussed in *Chapter 1*, the impedance networks can be classified as magnetic-coupled-based and non-magnetic-coupled-based. In this chapter, three modified DC-DC converters with ISNs are introduced.

As shown in Fig. 3.1, a modified switched-capacitor quasi-Z-source (SC-qZS) converter as a non-magnetic-coupled-based topology with continuous input currents is proposed by demonstrating the detailed theoretical analysis [J5], [81]. It can achieve high conversion ratios and low voltage stresses across the components [J5], [81]. Moreover, it can be observed that the SC-qZS is similar to the topologies presented in *Chapter 2* as the non-magnetic-coupled-based topology. Hence, their operation principles are similar and detailed analysis related to this topology is not explored in this chapter.

Additionally, the magnetic-coupled-based DC-DC converters with ISNs are promising solutions due to their high voltage gains and low component counts. Therefore, a modified trans-inverse coupled-inductor single-ended primary-inductor (SEPIC) converter (TICSC) and a modified Y-source converter (MYSC) are presented in this Chapter [J3, J4], [82, 83]. The high conversion ratios are obtained by applying coupled inductors to the ISNs. Furthermore, the operation principle in continuous conduction mode (CCM), the benchmarking various DC-DC converters, and experimental results are provided to validate the proposed converters in this chapter.

3.1 Trans-Inverse Coupled-Inductor SEPIC Converter

Fig. 3.2 shows a modified trans-inverse coupled-inductor SEPIC converter (TICSC) [J3], [82]. The TICSC is obtained by replacing the intermediate inductor of the conventional SEPIC with an ISN, which includes one diode (D_1), one capacitor (C_1) and coupled inductors with an n-turns-ratio [J3], [82]. Moreover, it also includes an inductor (L), one power switch (S_i), one output diode (D_2) and two capacitors (C_2 and C). Several features of the TICSC can be summarized as [J3], [82]

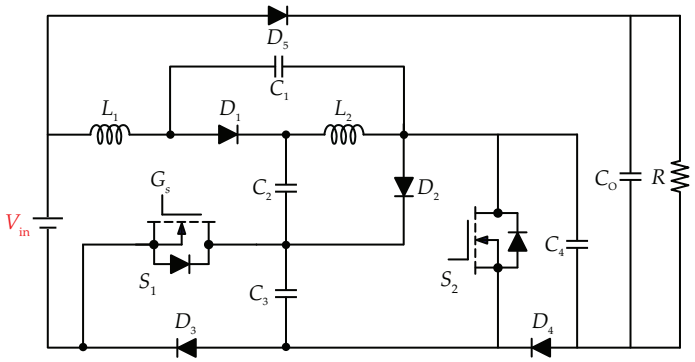


Fig. 3.1: Schematic of the proposed switched-capacitor quasi-Z-source DC-DC converter [J5], [81].

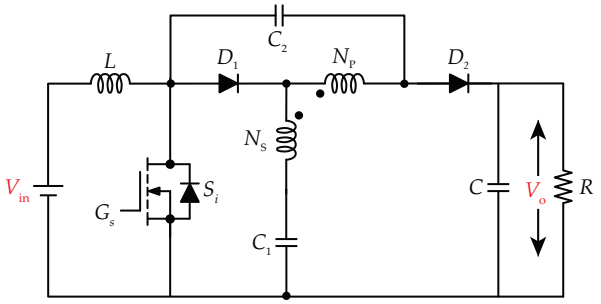


Fig. 3.2: Schematic of the proposed trans-inverse coupled-inductor SEPIC DC-DC converter (TICSC) [J3], [82].

- The trans-inverse capability can be obtained because the improved boosting capability of the TICSC can be obtained by decreasing the turns-ratio of the coupled-inductor.
- The TICSC operates with a large flexible duty cycle range ($0 < D < 1$).
- The TICSC can be applied in the renewable energy systems due to the continuous input current.
- Possible DC current saturation in the core can be overcome by adding a capacitor to the primary winding.

3.1.1 Operation Principle in the CCM Mode

The operation of the TICSC comprises two stages, which is identical to that of the impedance-source inverters. The equivalent circuits under the steady-state condition are shown in Fig. 3.3.

In Fig. 3.3(a), the power switch S_i receives the turn-on signal, so that the diodes D_1 and D_2 are in OFF-state. Meanwhile, the input inductor is charged by the DC source, and the output capacitor supplies the power to the output load, which is isolated from

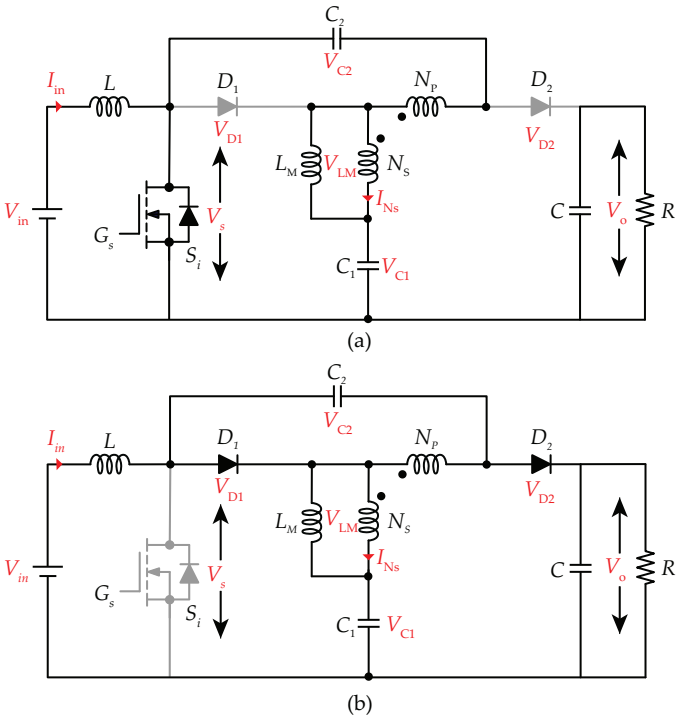


Fig. 3.3: Operation modes of the TICSC if S_i is: (a) ON-stata, and (b) OFF-state [J3], [82].

the converter [J3], [82]. According to Fig. 3.3(a), the input inductor voltage and leakage inductance voltage can be indicated as

$$V_L = V_{\text{in}} \tag{3.1}$$

$$V_{\text{LM}} = \frac{V_{\text{C1}} - V_{\text{C2}}}{n-1}. \tag{3.2}$$

Fig. 3.3(b) presents the other operation state, where S_i is turned OFF, and D_1, D_2 are in ON-state. Thus, the load side can receive the energy which is reserved in the input inductor. Similarly, the input inductor voltage and leakage inductance voltage in this stage can be written as

$$V_L = V_{\text{in}} + V_{\text{C2}} - V_o \tag{3.3}$$

$$V_{\text{LM}} = \frac{V_{\text{C1}} - V_{\text{O}}}{n-1} \tag{3.4}$$

To obtain the voltage gain G, the volt-second balance principle can be applied to L and L_M as

$$DV_{\text{in}} + (1-D)\left(V_{\text{in}} - V_{\text{C2}} - V_o\right) = 0 \tag{3.5}$$

$$D\left(\frac{V_{\text{C2}} - V_{\text{C1}}}{n-1}\right) + (1-D)\left(\frac{V_{\text{C1}} - V_o}{n-1}\right) = 0. \tag{3.6}$$

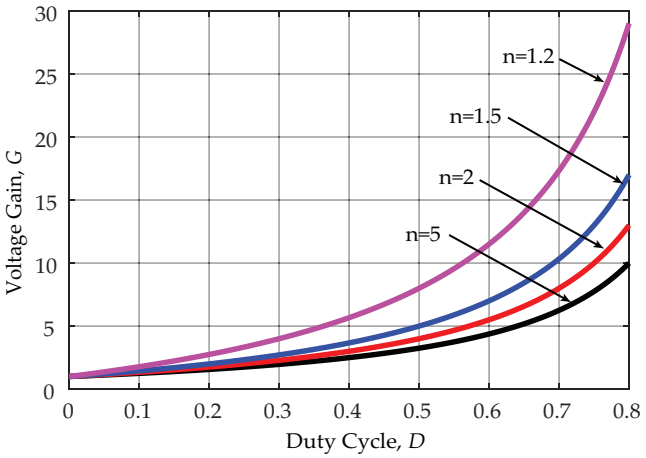


Fig. 3.4: Variation of voltage gain versus duty cycle in the proposed TICSC in Fig. 3.2 [J3], [82].

After further simplifications, the capacitor voltages and output voltage can be expressed as

$$V_{C1} = \left(1 + \frac{nD/(n-1)}{1-D}\right) \cdot V_{in} \tag{3.7}$$

$$V_{C2} = \left(\frac{nD/(n-1)}{1-D}\right) \cdot V_{in} \tag{3.8}$$

$$V_o = G \cdot V_{in} = \left(\frac{1+nD/(n-1)}{1-D}\right) \cdot V_{in} \tag{3.9}$$

According to Eq. (3.9), the relationship considering the duty cycle, turns-ratio and voltage gain is obtained, which is shown in Fig. 3.4 [J3], [82]. It is clear that the trans-inverse capability is achieved, where decreased turns-ratio leads to a higher voltage gain. Additionally, the TICSC operates under a wide adjustable duty cycle range compared with other similar topologies, which will be verified in the following subsections.

3.1.2 Comparison Analysis

To present the unique features of the TICSC, trans-inverse converters in [84–86], Γ-source converter in [65], Y-source converter in [67], improved-Γ-source converter in [66] are compared with the proposed TICSC. Table 3.1 summarizes the comparison results as regards to the component count, characteristics of the input current, switch voltage stress and duty cycle range. According to Table 3.1, the Γ-source converter and Y-source converter have fewer components compared with other converters. However, they cannot attain a continuous input current because of the input diode, so that the performance of the converters may be degraded because of the large input ripples in PV or fuel cell systems. Additionally, the input currents of the converters in [84] and [66] are continuous with low ripples. However, the limitation of the two converters is

Table 3.1: Comparison of the TICSC with Other Selected Coupled-Inductor-Based Topologies [J3], [82]

Converter	Trans-inverse [84]	Γ-source [65]	Y-source [67]	Γ-source [66]	Trans-inverse [85]	Trans-inverse [86]	TICSC
No. of inductors+ couple inductors	1+2	0+2	0+3	1+2	1+2	0+2	1+2
No. of capacitors	5	2	2	3	5	3	3
No. of switches	1	1	1	1	1	1	1
No. of diodes	4	2	2	2	4	3	2
Input current ripple	low	high	high	low	low	high	low
Block capacitor	yes	yes	yes	yes	no	no	yes
Switch voltage stress	$\frac{n-1}{2(n-1)+D}$	1	1	1	$\frac{n-1}{2n-1}$	$\frac{n-1}{2n-1}$	$\frac{n-1}{2n-1}$
Duty cycle range	$0<D<\frac{n-1}{n}$	$0<D<\frac{1}{1+\frac{1}{n-1}}$	$0<D<\frac{1}{k}$	$0<D<\frac{1}{2+\frac{1}{n-1}}$	$0<D<\frac{n-1}{2n-1}$	$0<D<1$	$0<D<1$

that both cannot operate within a wide adjustable control range. It should be noted that the switch voltage of the converters in [65–67] is the same as the output voltage, which increases the cost of the component due to high voltage stress. Although the converter in [86] has a wide control range, an additional filter is required to eliminate the high input current ripples. However, in the TICSC, the current ripple is very low and only two diodes are employed. Additionally, the core saturation problem is addressed thanks to the dc current block capacitor in a direct connection to the winding [J3], [82]. Moreover, the wider D variation range of the TICSC makes it suitable for any turns-ratio of the coupled inductor, thus reducing the sensitivity to the D. In addition, the TICSC achieves lower voltage stresses compared to the converters in [65–67]. As exemplified in Fig. 3.5, the D of the converters in [84, 85] is limited to a narrow range in comparison to the TICSC converter. Thus, the TICSC operates in a wider range which simplifies the overall control.

3.1.3 Experimental Results

Fig. 3.6 presents the hardware prototype, which can be used to validate the proposed TICSC. The detail parameters are presented in Table 3.2. As indicated in Fig. 3.7, the experimental results are obtained with the output power being 168 W and 325 W, respectively. Fig. 3.7 shows that the output voltage is boosted from 48 V to 400 V under an open-loop control. In Fig. 3.7(a), the average input current is about 3.5 A. Additionally, the continuous input current with low ripples can be observed in Fig. 3.7(a) as expected [J3], [82].

As for the switch voltage, it is only 130 V and much lower compared with V_o (400 V) [J3], [82]. Furthermore, it should be noted that no high voltage spikes can be observed on the power switch, which validates the previous analysis. According to the secondary current (I_{Ns}) waveform in Fig. 3.7, there is no dc current due to the series capacitor C_1, which is preventing from the core saturation. Fig. 3.7(b) presents the

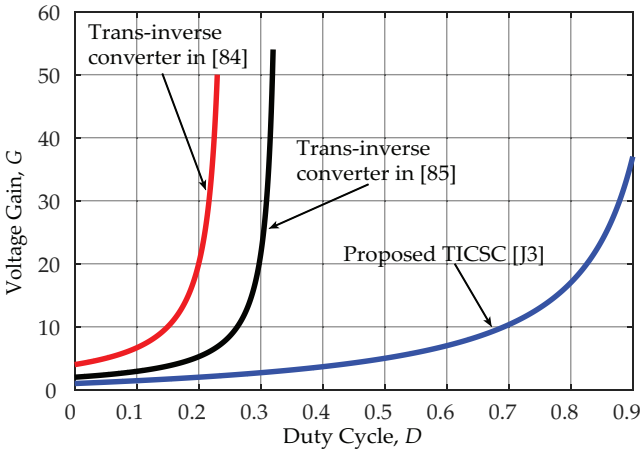


Fig. 3.5: Variation of voltage gain versus duty cycle in the proposed TICSC and converters in [84, 85] for n = 1.5 [J3], [82].

Table 3.2: Parameters and Selection of the TICSC Components [J3], [82]

Parameter/Decription	Symbol	Value/Part Number
Power rating	P	150-400 W
Input/Output voltage	V_{in}/V_o	48/400 V
Capacitor/input inductance	C, C_1, C_2/L	100 μF/640 μH
Turn ratio	n	28:20 Core:B66397G0000X197
Leakage/magnetizing inductance	L_{leakage}/L_M	1.27/220 μH
Switching frequency	f_s	100 kHz
Duty Cycle	D	0.62
Switch	S_i	IPP60R099C6XKSA1
Diode	D_1&D_2	IDP30E65D2XKSA1

experimental results with the output power being 325 W. It is clear in Fig. 3.7(b) the output voltage is 396.3 V. That is, the boosting capability is not affected by the leakage inductance. Moreover, the peak diode voltage V_{D2} is also 130 V, which is the same as switch voltage.

The efficiency of the TICSC is obtained under a wide range from 50 to 400 W, as presented in Fig. 3.8 [J3], [82]. The overall efficiency is above 92% and the maximum efficiency can reach 94% at the full load condition [J3], [82]. The loss distribution of the TICSC with 325 W output power is shown in Fig. 3.9. The majority of the power losses are from the inductive components. The power loss related to the power switch also accounts for about 29%, which is much higher than the loss related to the diodes or other losses. Therefore, to improve the efficiency of the prototype, the inductors with advanced material and gallium nitride (GaN)/Silicon carbide (SiC) devices could be employed.

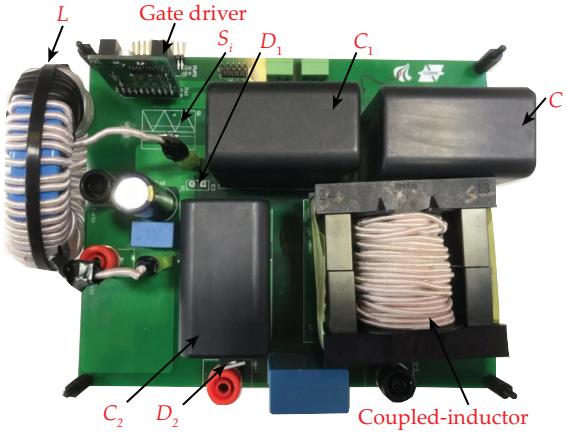


Fig. 3.6: Experimental prototype of the proposed EICSC [J3], [82].

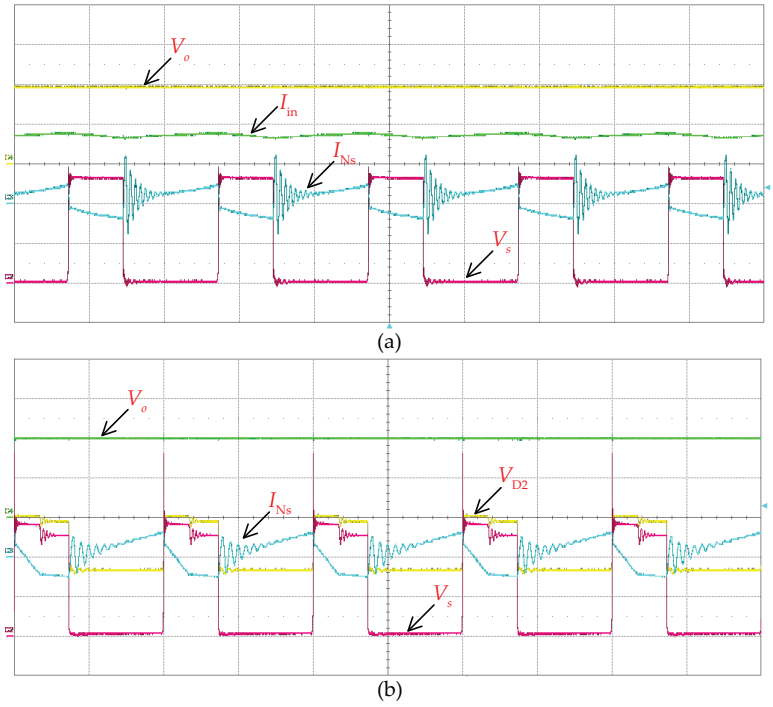


Fig. 3.7: Experimental results under two output power conditions: (a) output power: 168 W and (b) output power: 325 W (output voltage (200 V/div), input current (5 A/div), switch voltage (50 V/div) and coupled inductor secondary current (5 A/div) and diode D_2 voltage (100 V/div)) [J3], [82].

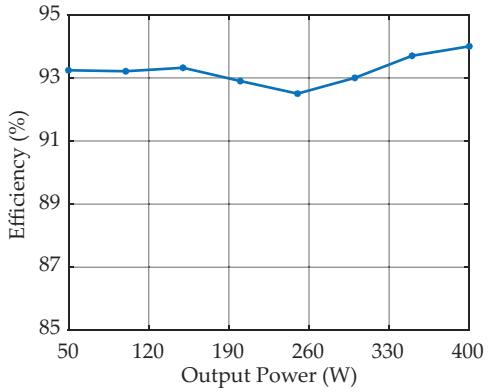


Fig. 3.8: System efficiency of the proposed EICSC (V_{in}=48 V, V_o=400 V, D=0.62, f_s=100 kHz) [J3], [82].

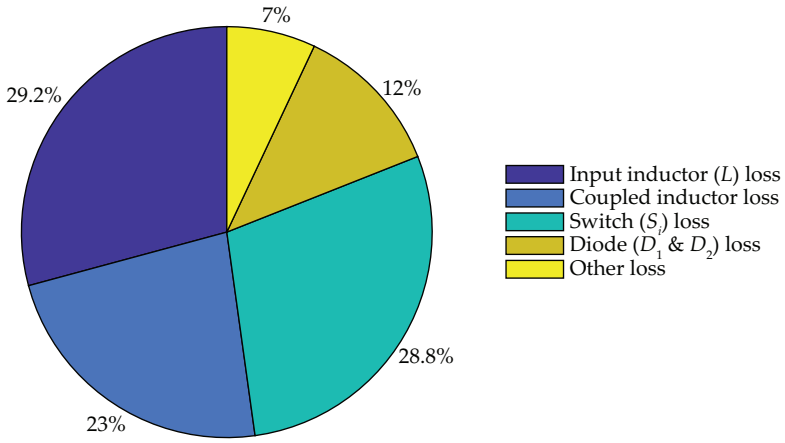


Fig. 3.9: Power loss distribution of the TICSC at 325 W output power [J3], [82].

3.2 Modified Y-Source DC-DC Converter

A modified Y-source DC-DC converter (MYSC) with large conversion ratios and low switch stress was proposed in [J4], [83]. It also features continuous input currents and wide adjustable control ranges [J4], [83]. Moreover, the large conversion ratios are obtained by using low turns-ratios, while the core saturation problem can be overcome by applying a dc-current-blocking capacitor [J4], [83].

Fig. 3.10 indicates the schematics of the MYSC. In Fig. 3.10, the converter has an input inductor (L), a power switch (S_i), two diodes (D_1, D_2), three capacitors (C, C_1, C_2) and a coupled-inductor with three windings (the turns-ratios are defined as N_1, N_2 and N_3) [J4], [83]. It is clear in Fig. 3.10 that S_i is relocated from the output dc-link side (HV) to the input source side (LV) compared with the original Y-source converter, resulting in lower voltage stress on the switch [J4], [83]. Furthermore, the inductor

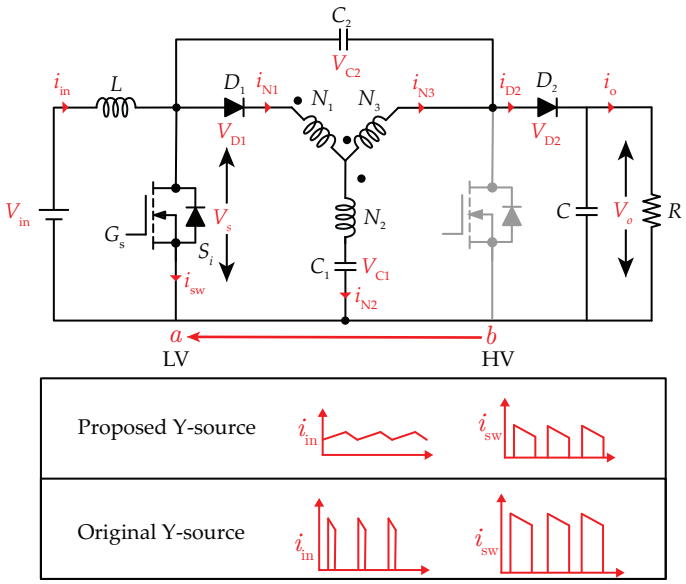


Fig. 3.10: Schematic of the modified Y-source converter (MYSC) in contrast to the original Y-source converter [J4], [83].

current of the MYSC can be maintained to be continuous due to an extra input inductor and the peak current of the power switch is also reduced.

3.2.1 Operation Principle

The operation principle analysis could be conducted under the following assumptions:

- The parasitics of the switch are not taken into account in the analysis.
- The capacitors are large enough to maintain a constant value.
- The leakage inductance of the coupled inductor is not considered.

The equivalent circuits of the MYSC under two operation states are presented in Fig. 3.11, where the magnetizing inductance L_m is included. The input voltage, inductor voltage, capacitor voltages and magnetizing inductance voltage are denoted as V_{in}, V_L, V_{C1}, V_{C2}, and V_{Lm}. For the three windings, their corresponding voltages V_{N1}, V_{N2}, V_{N3} and V_{Lm} are expressed as

$$V_{\text{N1}} = V_{\text{Lm}}, \qquad V_{\text{N2}} = \frac{N_2}{N_1} V_{\text{Lm}}, \qquad V_{\text{N3}} = \frac{N_3}{N_1} V_{\text{Lm}}. \tag{3.10}$$

In Fig. 3.11(a), S_i is turned ON, and the voltage source charges the inductor [J4], [83]. The current follows loop ① in Fig. 3.11(a). Meanwhile, both diodes are in OFF-state and the load R can be supplied by the capacitor C. When applying the KVL to the loop ①, it can be obtained that

$$V_L - V_{\text{in}} = 0 \tag{3.11}$$

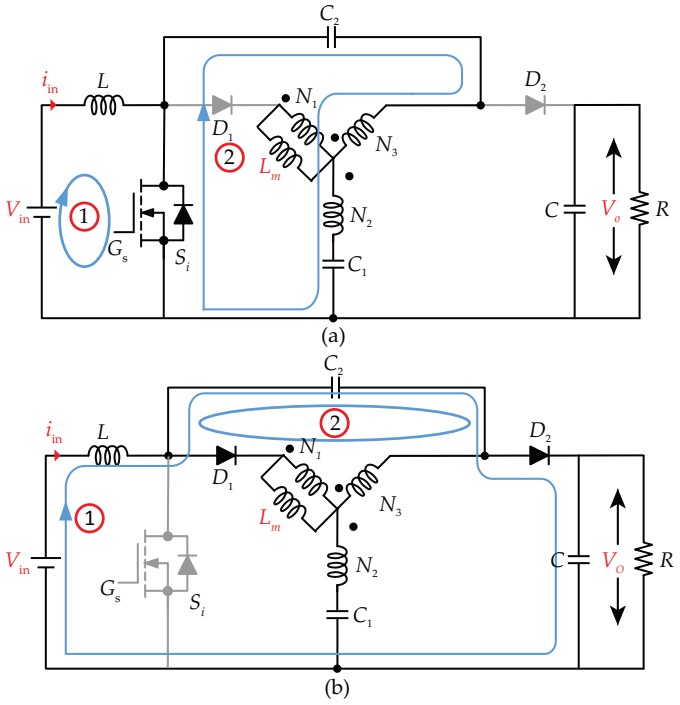


Fig. 3.11: Operation modes of the MYSC with switch S_i being: (a) turn-ON, and (b) turn-OFF [J4], [83].

$$-V_{C2} - V_{N3} + V_{N2} + V_{C1} = 0 \tag{3.12}$$

By substituting (3.10) into (3.11), the voltage of the magnetizing inductance can be expressed as

$$V_{Lm} = \frac{N_1}{N_3 - N_2}\left(V_{C1} - V_{C2}\right) \tag{3.13}$$

During the state in Fig. 3.11(b), S_i is turned OFF and the inductor releases the previously-stored energies to the load. Similarly, the equations for loop ② are attained as

$$-V_L + V_{in} + V_{C2} - V_o = 0 \tag{3.14}$$

$$-V_{C2} - V_{N3} - V_{N1} = 0 \tag{3.15}$$

By Substituting (3.10) into (3.15), V_{Lm} is given as

$$V_{Lm} = -V_{C2}\frac{N_1}{N_3 + N_1} \tag{3.16}$$

By applying the voltage-second principle to the inductors L and L_m [J4], [83], i.e., Eqs. (3.11), (3.13), (3.14), (3.16), it can be obtained that

$$DV_{in} + (1 - D)\left(V_{in} + V_{C2} - V_o\right) = 0 \tag{3.17}$$

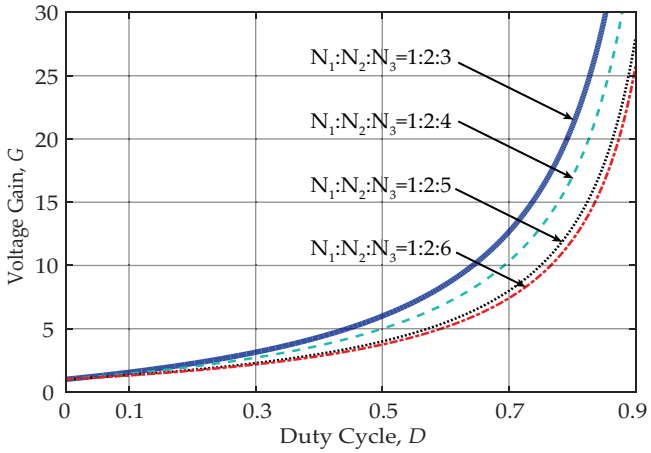


Fig. 3.12: Variation of voltage gain versus duty cycle in the MYSC with various winding ratios [J4], [83].

$$D\frac{N_1\left(V_{C1}-V_{C2}\right)}{N_3-N_2}+(1-D)\left(-\frac{N_1}{N_1+N_3}V_{C2}\right)=0 \tag{3.18}$$

Furthermore, the expressions regarding V_{C1} and G are indicated as

$$V_{C1}=V_{in}+V_{C2}=\left(1+\frac{KD}{1-D}\right)V_{in} \tag{3.19}$$

$$G=\frac{V_o}{V_{in}}=\frac{1+DK}{1-D} \tag{3.20}$$

where the winding factor K is expressed as [J4], [83]

$$K=\frac{N_3+N_1}{N_3-N_2} \tag{3.21}$$

It can be observed in Eq. (3.21) that N_3 should be larger than N_2 to ensure the boosting capability. As shown in Fig. 3.12, the MYSC could attain higher voltage gains by utilizing a lower turns-ratio if the duty cycle is the same, which leads to a smaller size and cost of the power converter.

3.2.2 Design Considerations

The winding currents i_{N1}, i_{N2} and i_{N3} through the coupled inductors can be expressed as

$$i_{N1}=\frac{N_3}{N_1}i_o, \qquad i_{N2}=0, \qquad i_{N3}=i_o \tag{3.22}$$

where i_o is the output current. By following the KCL to the circuit, the magnetizing current i_{Lm} is expressed as

$$i_{Lm}=i_{N1}+i_{N3}=(1+\frac{N_3}{N_1})i_o \tag{3.23}$$

During the ON-state as shown in Fig. 3.11(a), i_{N_2} and i_{N_3} are equal:

$$i_{\mathrm{N1(ON)}} = i_{\mathrm{N3(ON)}} \tag{3.24}$$

According to the ampere-turn balance for the transformers, we have

$$N_1 i_{\mathrm{N1}} + N_2 i_{\mathrm{N2}} = N_3 i_{\mathrm{N3}} \tag{3.25}$$

Then, substituting (3.23) and (3.24) into (3.25) gives

$$i_{\mathrm{N2(ON)}} = i_{\mathrm{N3(ON)}} = \frac{N_1}{N_3 - N_2} i_{\mathrm{N1(ON)}} \tag{3.26}$$

In addition, i_{N_2} flows through C_1 and i_{N_3} flows through C_2. Accordingly, the capacitor voltage ripples are expressed as

$$\Delta v_{C_1} = \frac{N_1 i_{Lm}}{N_3 - N_2} \cdot \frac{D}{C_1 f}, \Delta v_{C_2} = \frac{N_1 i_{Lm}}{N_3 - N_2} \cdot \frac{D}{C_2 f} \tag{3.27}$$

where f represents the switching frequency. And then, (3.27) can be used to calculate the capacitance. Furthermore, the output capacitor C is expressed as

$$C = \frac{i_o D}{\Delta v_C f} \tag{3.28}$$

where Δv_C represents the required capacitor voltage ripple. The design of the coupled inductor can be followed by the design principles proposed in [67], and then the minimum magnetizing inductance L_m is calculated as [J4], [83]

$$L_m = \frac{N_1 \left(V_{C2} - V_{C1}\right) D}{2 i_o \left(1 + \frac{N_3}{N_1}\right) \left(N_3 - N_2\right) f} \tag{3.29}$$

3.2.3 Voltage Stress Analysis

This section provides a detailed analysis of the voltage stresses across the components. With this analysis, the proper components can be selected.

When S_i is switched OFF as presented in Fig. 3.11(b), the voltage V_{sw} across the switch can be obtained as

$$V_{\mathrm{sw}} = V_o - V_{\mathrm{C2}} \tag{3.30}$$

By substituting (3.19) and (3.20) into (3.22), the voltage stress are indicated as

$$\frac{V_{\mathrm{sw}}}{V_{\mathrm{in}}} = \frac{G + K}{1 + K} = \frac{1}{1 - D} \tag{3.31}$$

It is known from Eq. (3.31) that the ratio of the switch stress is exclusively related to the duty cycle if the input voltage maintains a constant value [J4], [83]. Moreover, when S_i is turned ON, the ratios of the diode stresses are expressed as

$$\frac{V_{\mathrm{D1}}}{V_o} = \frac{K^2 + KG + 2K}{1 + KD}, \qquad \frac{V_{\mathrm{D2}}}{V_{\mathrm{in}}} = \frac{G + K}{1 + K} \tag{3.32}$$

Based on the above analysis, the proper sized semiconductors can be selected with the required winding factor K in Eq. (3.21) and output voltage. Finally, the capacitor stresses can be obtained based on Eq. (3.19) as

$$\frac{V_{\mathrm{C1}}}{V_{\mathrm{in}}} = \frac{KG + 1}{K + 1}, \qquad \frac{V_{\mathrm{C2}}}{V_{\mathrm{in}}} = \frac{KG - K}{K + 1} \tag{3.33}$$

Table 3.3: System Benchmarking of Selected Coupled Inductor Topologies [J4], [83]

Converters in	[87]	[88]	[89]	[65]	[66]	[67]	[68]	[71]	MYSC
Inductors + coupled inductors	0+2	1+2	4+0	0+2	1+2	0+3	1+3	2+3	1+3
Capacitors	4	5	1	2	3	2	3	5	3
Switches	1	1	2	1	1	1	1	1	1
Diodes	4	4	7	2	2	2	2	3	2
Current ripple	high	low	high	high	low	high	low	low	low
Duty cycle control range	$0<D<1$	$0<D<1$	$0<D<1$	$0<D<\frac{1}{1+\frac{1}{n-1}}$	$0<D<\frac{1}{2+\frac{1}{n-1}}$	$0<D<\frac{1}{K}$	$0<D<\frac{1}{K}$	$0<D<\frac{1}{K+2}$	$0<D<1$

Table 3.4: Benchmarking of Voltage Stresses across the Components between the prior-art Y-source converters and the proposed MYSC [J4], [83]

Voltage stress	Y-source [67]	quasi-Y-source [68]	Proposed MYSC [J4], [83]
C_1	$\frac{4G+1}{5}$	$\frac{4G+1}{5}$	$\frac{5G+1}{6}$
C_2	/	$\frac{4G-4}{5}$	$\frac{5G-5}{6}$
D_1	$4G$	$4G$	$\frac{4G+25}{6}$
D_2	G	G	$\frac{G+5}{6}$
S	G	G	$\frac{G+5}{6}$

3.2.4 Comparison with Selected Topologies

Table 3.3 presents a comparison between the MYSC and the other similar topologies with coupled inductors. In the comparison, the turns-ratio is defined as n for all the two-windings inductor and the winding factor is K for all the three-winding inductors. By observing the component-count for the topologies, fewest components are utilized in the Γ-source converter among the selected topologies. Nevertheless, the continuous input current cannot be achieved in the Γ-source converter, which restricts its application. To tackle this problem, an improved Γ-source converter was proposed in [66]. However, its control range is very limited and the duty cycle cannot be adjusted within a wide range. The modified Y-source converter in [71] utilizes more components for a higher voltage gain, which increases the overall cost to some extent. As observed in Fig. 3.13, the voltage gains of the selected converters are comparatively larger than that of the MYSC, and however, the limited range of the duty cycle hinders its further application. That is, the control is sensitive to the variation of the duty cycle for high conversion ratios [J4], [83]. Compared to the MYSC, the converters in [87–89] can also be operated with a wide control range. Additionally, the input current ripple of the converters in [87] and [89] is relatively high in comparison to the MYSC.

To investigate the voltage stress performance regarding the capacitor, diodes, and switches among the Y-source converter [67], quasi-Y-source converter [68] and the MYSC, a comparison under the same winding factor ($K = 5$) is performed and summarized in Table 3.4 [J4], [83]. Table 3.4 shows that although the topology is modified by relocating the power switch, the capacitor voltage stress is almost the same and not influenced by the rearrangement of the switch [J4], [83]. However,

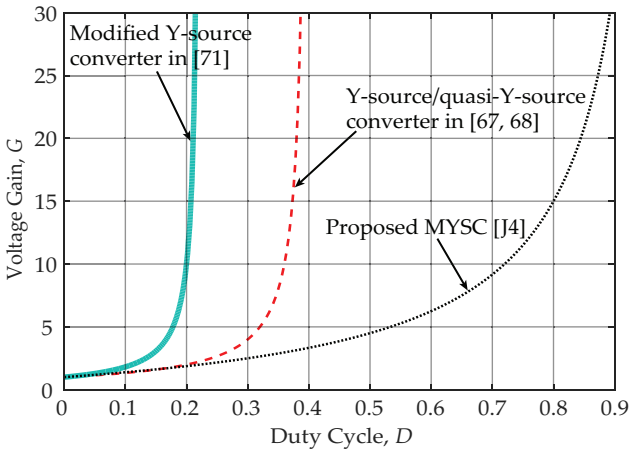


Fig. 3.13: Variation of voltage gain versus duty cyle of the MYSC and prior-art converters by employing the same winding ratios [J4], [83].

Table 3.5: Parameters and Selection of the MYSC Components [J4], [83]

Parameter/Description	Symbol	Value/Part Number
Rated Power	P	250 W
Input/Output Voltage	V_{in}/V_o	40/400 V
Capacitor/Input Inductor	C, C_1, C_2/L	100 μF/640 μH
Turns-Ratio	$N_1 : N_2 : N_3$	20:12:20
Core	/	B66397G0000X197
Switching Frequency	f_s	100 kHz
Duty Cycle	D	0.60
Switch	S_i	IPP60R099C6XKSA1
Diode	D_1&D_2	IDP30E65D2XKSA1

the voltage stresses across the diodes and power switch in the MYSC are reduced considering the relocation of the power switch, which is beneficial in reducing the costs when a fairly high dc output voltage is needed.

3.2.5 Experimental Verification

To validate the MYSC, the prototype of the MYSC is fabricated and the key parameters are listed in Table 3.5. In order to reduce the adverse impact of the leakage inductance, the windings of the coupled inductor are designed in an interleaved structure with 20, 12 and 20 turns. The winding factor K is, therefore, equivalent to 5. The expected voltage gain is 10 with the duty cycle being 0.6.

In Fig. 3.14, V_o is around 390 V, which is consistent with the theoretical value (e.g., 400 V). Moreover, in Fig. 3.14, the average value of the continuous input current is about 5.4 A with low ripples. That is, the continuous input current can be obtained from the dc source. Additionally, the winding current I_{N2} is a periodic signal without DC currents, because the magnetic core saturation problem is solved by adding the

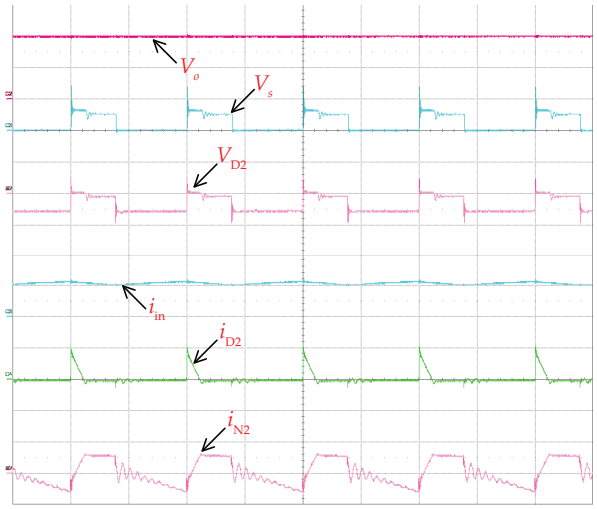


Fig. 3.14: Experimental results of the MYSC operating at 200 W (output voltage V_o [200 V/div], switch voltage V_S [200 V/div], voltage of D_2-V_{D2} [200 V/div], input current i_{in} [5 A/div], current of D_2-i_{D2} [10 A/div], secondary current i_{N2} [10 A/div], time [5 μs/div]) [J4], [83].

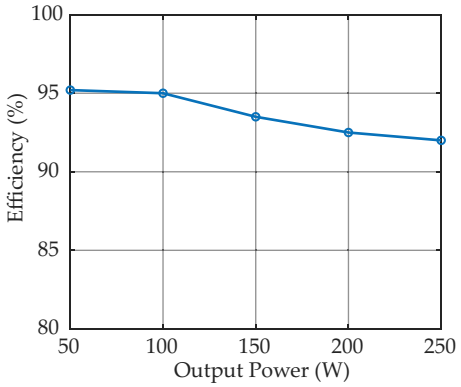


Fig. 3.15: Measured efficiency of the modified Y-source converter [J4], [83].

capacitor C_1 to the winding N_2 [J4], [83]. Furthermore, the peak switch voltage is only 110 V, which is about a quarter of the output voltage. Similarly, the peak diode voltage V_{D2} is also about 110 V. It is worth mentioning that D_2 can achieve zero current switching (ZCS), as observed in Fig. 3.14 (the diode current I_{D2}), which can result in fewer power losses from the diode.

The efficiency under different output power levels is measured and indicated in Fig. 3.15. The input voltage is a constant of 40-V and the converter operates within the range from 50 W to 250 W.

Fig. 3.15 indicates that the system efficiency of the MYSC is over 92% and the peak efficiency is 95.2% [J4], [83]. In addition, Fig. 3.16 shows the power loss distribution

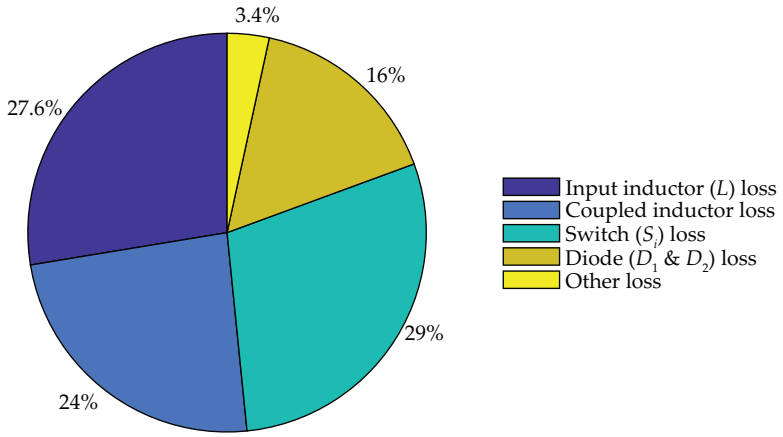


Fig. 3.16: Power loss distribution of the modified Y-source DC/DC converter at 250 W output power [J4], [83].

of the MYSC. As shown in Fig. 3.16, the majority of power losses are from the input inductor, the coupled inductor and the power switch. Thus, to obtain a better performance in terms of system efficiency, advanced core material and efficient power devices could be utilized.

3.3 Summary

In this chapter, several modified impedance-source DC-DC converters are introduced. The TICSC and MYSC are both developed based on the coupled inductor. Compared to various DC-DC converters, the TICSC and MYSC both features continuous input current, trans-inverse capability and wide adjustable duty cycle range. In addition, the possible DC current saturation in the core is addressed by the configuration of the circuit topology. And then, the benchmarking results are provided and two prototypes have been built to validate the performance of the TICSC and MYSC.

Chapter 4

4 Design and Optimization of Impedance-Source Network

Although many efforts have been made to improve the performance of ISNs regarding novel topologies, design and optimization of the ISN have not been fully addressed yet. Seen from the design perspective, the performance of ISNs can be further enhanced. Therefore, this section presents a systematic design procedure to optimize the components of ISNs (e.g., inductors and capacitors) in a way to maximize the performance. Especially, special design considerations for ISNs are explored: topologies, modulation strategies, switching frequencies, and practical layout optimization. Case studies are conducted to validate the proposed design procedure and considerations.

4.1 Design Considerations

In order to systematically design of ISNs, certain parameters should be considered. Therefore, the following design considerations in terms of topologies, modulation strategies, switching frequencies, and practical layout optimization are reported [C4], [90].

4.1.1 Topologies

To select the proper ISN topology based on different requirements and applications, several design concerns regarding the boosting ratios, input current ripples, stresses across the components, and duty cycle range should be taken into account. As shown in Fig. 4.1, the ISN topologies discussed in *Chapter* 1 can be classified as several groups based on the variation range of the voltage gains [C4], [90]. The basic ZSI/qZSI topologies are suitable for the applications where the boosting ratio ranges from 1 to 2. Furthermore, for the application of renewable energy, the qZSI is a more promising candidate than the ZSI because of its feature of the continuous input current. Furthermore, the demand for capacitance in the qZSI is much lower in contrast to the ZSI [91]. If a higher boosting ratio is required, the switched-inductor, diode-assisted, capacitor-assisted ZSI/qZSI could be further employed. Compared to the basic ZSI/qZSI, they have a better boosting capability by adding more components.

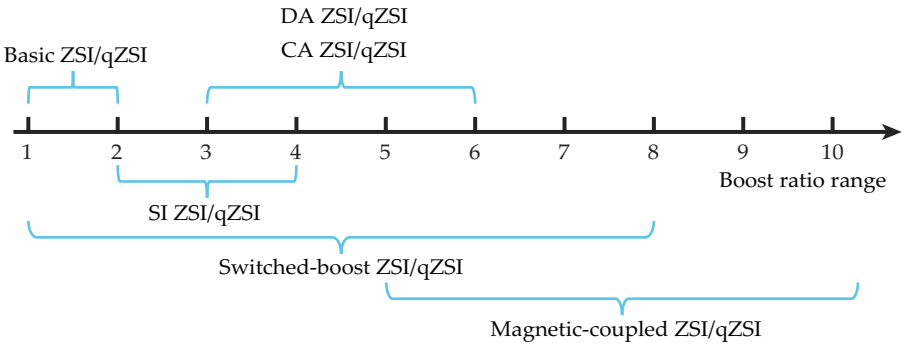


Fig. 4.1: Categories of impedance-source networks based on different voltage gains [C4], [90].

Moreover, the ZSI/qZSI with additional switched-boost networks can operate under a wide voltage gain range. Additionally, for example, microinverters in PV applications usually require high boosting ratios (larger than 5), where the magnetic-coupled ZSI/qZSI is a suitable alternative. A summary of different categories of impedance-source topologies is reported in [C4], [90], which addresses the main advantages, disadvantages and appropriate applications.

4.1.2 Modulation Strategies

By modifying the conventional PWM algorithms, three classic PWM methods, i.e., simple boost control (SBC) [18], maximum boost control (MBC) [92], and maximum constant boost control (MCBC) [93] can be applied to the systems with ISNs [20].

In the SBC method, the ST interval during one switching period is constant and there is no ripple related to the output frequency [18]. Nonetheless, the SBC may lead to higher voltage stresses over switches compared with the MBC and MCBC [20]. To counter this, the MBC was introduced, which applies the ST states to replace the normal zero states [92]. Nevertheless, the ST duty cycle in the case of the MBC cannot be a fixed value, which may induce the low-frequency ripples to the components [92]. Accordingly, if the MBC is used as the modulation algorithm, the ISN-based systems have a higher requirement of capacitors and inductors, assuming the output frequency is low [C4], [90]. To reach a compromise between the SBC and the MBC, the modified modulation algorithm, the MCBC, was introduced in [93].

4.1.3 Switching Frequencies

In general, the switching frequency is decided by comparing different types of power devices and applications. In the initial phases, the prototypes of the ZSI/qZSI are primarily implemented by utilizing the insulated-gate bipolar transistor (IGBT) modules. Therefore, high power density of the whole system is difficult to reach. Thereby, the implementation of the silicon carbide (SiC) and gallium nitride (GaN) devices could greatly improve the performance of the ZSI/qZSI concerning the power density [19]. That is, the size of the inductors can be significantly reduced if a higher

switching frequency is employed. Moreover, the power loss should be considered to obtain a proper switching frequency. In [91], the concept of critical frequency was introduced, which provides a useful guideline for switching frequency selection, where a tradeoff between the efficiency and power density can be made.

4.1.4 Inductor Design

The inductors in the ZSI/qZSI systems are utilized to reduce the current ripples in the ST state [C4], [90]. According to the previous analysis regarding the operation principle, the inductor currents are increasing during the ST state, where the peak ripple can be obtained at the end of the ST state. Furthermore, on the basis of the given high-frequency peak-to-peak current ripple (e.g., ranging from 10% to 30% of the maximum inductor current), the inductors can be calculated under a specific modulation method [C4], [90]. Accordingly, the inductance can be obtained as

$$L = \frac{V_L \Delta T}{\Delta I_L} \tag{4.1}$$

where ΔT is the ST time, ΔI_L is the peak-to-peak current ripple, and V_L is the inductor voltage. Furthermore, the inductor design can be optimized by using coupled inductors. In the ZSIs, the currents through the two inductors are identical. Therefore, they can be built on the same toroidal core to obtain a double-inductance inductor and thereby reduce the size of the inductors in the ZSIs. The detailed design process for the coupled-inductor was reported in [94]. This may be extended to other ISNs by using coupled inductors to optimize the size and weight of the inductors. Additionally, the parasitics of coupled inductors are critical to the performance of the power converters. The optimization design of the coupled inductors by using interleaved structures could improve the performance of the converters, as reported in [C3], [95].

4.1.5 Capacitor Design

The optimization of the capacitance should also be taken into account in the ZSI/qZSI-based systems. The design criteria for the capacitors vary according to the system type (single-phase or three-phase). In three-phase ZSI/qZSI systems, the capacitors are generally applied to eliminate the current ripple and reduce the voltage ripple to be within a reasonable range [C4], [90]. Correspondingly, the capacitance can be obtained as

$$C = \frac{I_C \Delta T}{\Delta V_C} \tag{4.2}$$

where I_C is the capacitor current, and ΔV_C is denoted as voltage ripple with respect to the maximum capacitor voltage.

A major concern exists in the single-phase PV ZSI/qZSI systems, where the double–frequency power problem. So as to stop the double–frequency power into the PV panels, the input capacitors are normally placed parallel with the PV panel. However, the capacitors in the ZSI/qZSI can be utilized to tackle the double–frequency power [91, 96]. By building the AC equivalent model of the ZSI/qZSI, the relationship between the capacitance and the PV voltage ripple could be obtained [91, 96]. Then, the proper capacitor could be selected according to their relationship.

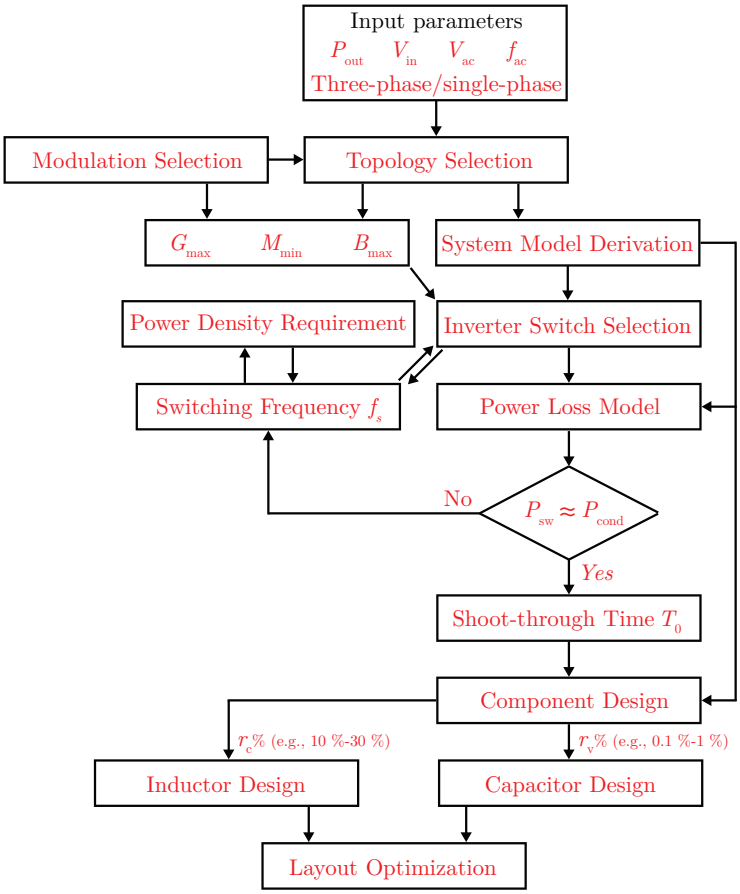


Fig. 4.2: Flowchart of the design procedure for impedance-source inverters [C4], [90].

4.2 Design Procedure

Fig. 4.2 indicates the flowchart of the design procedure based on the above-mentioned considerations. To implement this systematic design, the following parameters are required as the input parameters: P_{out}, rated power; V_{in}, input voltage; V_{ac}, output voltage (RMS); f_{ac}, grid frequency.

At first, the topology and corresponding modulation method should be selected based on the previous discussion, taking into account the appropriate voltage gain and particular application. In order to design the components and analyze the power loss, the system model should be derived under different operation states [91]. The variables related to the components can then be obtained. Furthermore, the maximum voltage gain G_{max} and boost factor B_{max}, and minimum modulation index M_{min} can be determined by a specific modulation control method. Then, the proper inverter switches can be selected based on the maximum voltage and current ratings. Furthermore, according to the power loss model derived from [91], the proper frequency can

Table 4.1: Specifications of the ZSI System [C4], [90]

Parameter	Value
Inductor L_1, L_2	290 μH
Capacitor C_1, C_2	34 μF
Switching frequency f_s	100 kHz
Input voltage V_{in}	$200 - 300$ V
Output voltage V_o	230 V
Rated power P_o	3 kW
Filter L_f	1.28 mH
Resistive load R_{load}	18 Ω

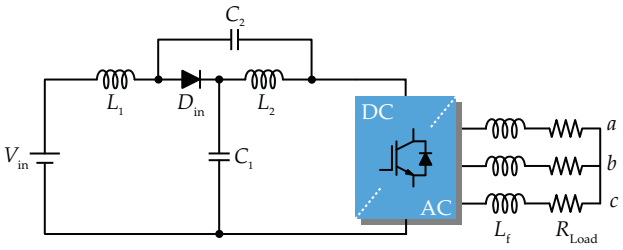


Fig. 4.3: Schematic of the three-phase quasi-Z-source inverter [C4], [90].

be determined by evaluating the switching loss and conduction loss under different switching frequency conditions. Accordingly, the derived ST time T_0 can be utilized to calculate the inductance and capacitance. Then, the optimization of the inductors and capacitors can be performed. At last, a practical layout design should be carried out for the final prototype. Compared with the conventional VSI, high voltage spikes across the power switches may be generated due to the stray inductance in the Z-source network. To address this, additional clamping circuits or minimization of the high-frequency commutation loop length could be applied in the ISNs [97].

4.3 Quasi-Z-Source Inverter Design

According to the above design procedure, a case study is demonstrated under the following specifications: the input voltage varies from 200 to 300 V, the system power rating is 3 kW, the output is set as a three-phase 50-Hz/230-V system with a resistive load [C4], [90]. Based on the input parameters, the required voltage gain should be in a range of 1 to 2. Therefore, the qZSI is a proper candidate as the main topology, as shown in Fig. 4.3. Moreover, the MCBC algorithm is utilized in the system due to its low voltage stress and low-frequency ripples [98]. Accordingly, the required minimum voltage gain G_{max} can be calculated as [C4], [90]

$$G_{\text{max}} = \frac{2\sqrt{2}V_{\text{ac}}}{\sqrt{3}V_{\text{in}}} = 1.88 \tag{4.3}$$

Afterwards, the voltage gain and boost factor is calculated as [C4], [90]

$$G = MB = \frac{M}{\sqrt{3}M - 1} \tag{4.4}$$

$$B = \frac{1}{\sqrt{3}M - 1} \tag{4.5}$$

Consequently, the minimum modulation index $M_{\min}$ and maximum boost factor $B_{\max}$ are calculated to 0.83 and 2.25. The duty cycle can be obtained as

$$D = 1 - \frac{\sqrt{3}M_{\min}}{2} = 0.273 \tag{4.6}$$

The maximum voltage stress V_s on the inverter bridge is

$$V_s = B_{\max} V_{\text{in}} = 2.25 \times 200 = 450 \text{ V} \tag{4.7}$$

In the meantime, the maximum inductor current is expressed as

$$I_{\text{in}} = \frac{P}{V_{\text{in}}} = \frac{3000}{200} = 15 \text{ A} \tag{4.8}$$

According to the power loss model presented in [91], the switching frequency can be selected as 100 kHz by considering the tradeoff between the efficiency and power density. The maximum ST time T_0 is

$$T_0 = \frac{D}{f_s} = 2.73 \ \mu s \tag{4.9}$$

In addition, the current ripple (r_i) and voltage ripple (r_v) are chosen as 20% and 0.1%. The inductance and capacitance can be calculated by

$$L_1 = L_2 = \frac{V_L \Delta T}{I_L r_i} = 290 \ \mu H \tag{4.10}$$

$$C_1 = C_2 = \frac{I_C \Delta T}{V_C r_v} = 34 \ \mu F \tag{4.11}$$

All the system parameters have been summarized in Table 4.1.

4.4 Optimal Design of the Coupled Inductors

In order to obtain a good performance of coupled-inductor-based converters, it is necessary to mitigate the side effects of the parasitics by optimizing the design of the coupled inductors [C3], [95]. Supposing that the coupled inductors are not in a good design, the unexpected operation states may happen, and the system performance is affected. For example, in the TICSCS, as discussed in *Chapter* 3, if a relatively large leakage inductance is present and considered, the operation states will be changed. It can be seen in Fig. 4.4 that the diode D_2 in the OFF-state before the end of the second stage. Thus, the three winding arrangements of the coupled inductors in the TICSC are explored in detail to illustrate their pros and cons in this Chapter. In addition, the simulation results based on the finite element analysis (FEA) are provided. At last, experimental tests are performed to verify the effectiveness of the TICSC by employing different designed winding arrangements.

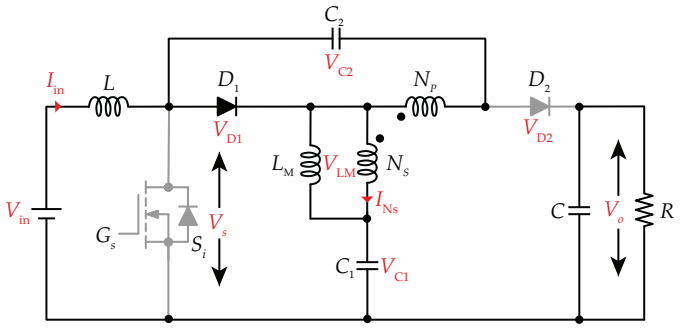


Fig. 4.4: Operation circuit of the MYSC if the diode D_2 is reverse-biased during the second stage [C3], [95].

4.4.1 Finite Element Analysis

To explore the parasitics of the coupled-inductor with different winding structures, FEA simulations are conducted. As indicated in Fig. 4.5, three different winding structures are explored, in which the turns-ratio for primary side (P) and secondary side (S) is set as 20:28 [C3], [95]. The specific winding architectures are listed in Table 4.2.

In Fig. 4.5(a), the P/S winding W_1 is presented in a non-interleaved way. It can be observed in Fig. 4.5(a) that the windings have three layers, where they have 20, 20, 8 turns, respectively. Furthermore, the winding (S/P/S) W_2 is designed in an interleaved structure in Fig. 4.5(b). In addition, Fig. 4.5(c) presents a more complicated interleaved structure W_3, where the windings of the first layer and second layer are distributed evenly, and the left secondary side turns are at the third layer. The magneto-motive force (MMF) distributions for these winding configurations are presented in Fig. 4.6.

Figs. 4.7(a)-(c) present the simulation results of the magnetic field energy for windings W_1-W_3. As shown in Fig. 4.6, the non-interleaved winding structure W_1 has a higher MMF than the winding structures W_2, W_3. Therefore, the more magnetic energy in the non-interleaved structures is reserved compared with interleaved structures. Accordingly, Fig. 4.7(a)-(c) show that the energy reserved in W_1 is higher than that of W_2 and W_3. Therefore, the non-interleaved structures have a larger leakage inductance in contrast to the interleaved structures. In addition, although W_2 and W_3 are both interleaved, the average MMF of W_3 is much smaller than that of W_2. That is, a more interleaved structure W_3 can ensure a lower leakage inductance.

Table 4.2: Coupled-Inductor Architectures [C3], [95]

Design	Build-up	Primary layer and turn	Secondary layer and turn
W_1	P/S	1 and 20	2 and 20/8
W_2	S/P/S	1 and 20	2 and 20/8
W_3	PS/SP/S	2 and 10/10	3 and 10/10/8

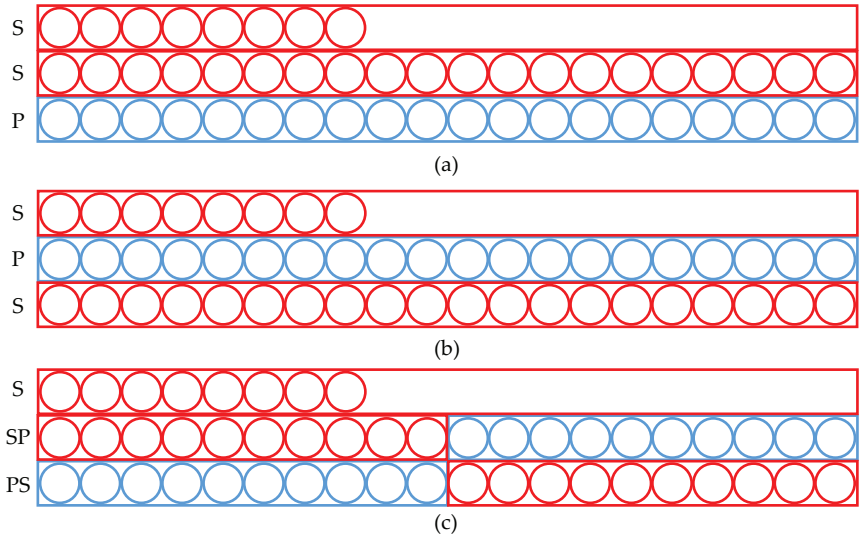


Fig. 4.5: Different winding configurations: (a) W_1, (b) W_2, and (c) W_3 [C3], [95].

Table 4.3: Parameters Comparison of the Winding Structures W_1,W_2 and W_3 for simulation and experiments [C3], [95]

	Leakage inductance		AC resistance	
	Simulation value	Measured value	Simulation value	Measured value
W_1	2.47 μH	4.3 μH	0.23 Ω	0.27 Ω
W_2	1.91 μH	3.33 μH	0.13 Ω	0.157 Ω
W_3	1.29 μH	1.8 μH	0.06 Ω	0.1 Ω

Moreover, to explore the AC resistance of the windings W_1, W_2, and W_3, Fig. 4.8 presents the current density for the three windings. According to the MMF distribution in Fig. 4.6, the maximum MMF from winding W_1 is much higher than windings W_2 and W_3. Therefore, the current density in the winding W_1 is much higher and not evenly distributed compared to the windings W_2 and W_3. That is, the interleaved windings W_2 and W_3 have lower AC resistance. Especially for the winding W_3, its field distortion is not as serious as the windings W_2 and W_3. Thus, the AC resistance in Fig. 4.8(c) can be reduced to some a large extent compared with those demonstrated in Figs. 4.8(a) and 4.8(b).

4.4.2 Experimental Verification

To validate the previous analysis, three coupled inductors with windings W_1, W_2, and W_3 are manufactured and experimental tests are performed. The duty cycle is 0.62, thus boosting the output voltage from 48 V to 400 V. The parameters of the setup are the same as those shown in Table 3.2.

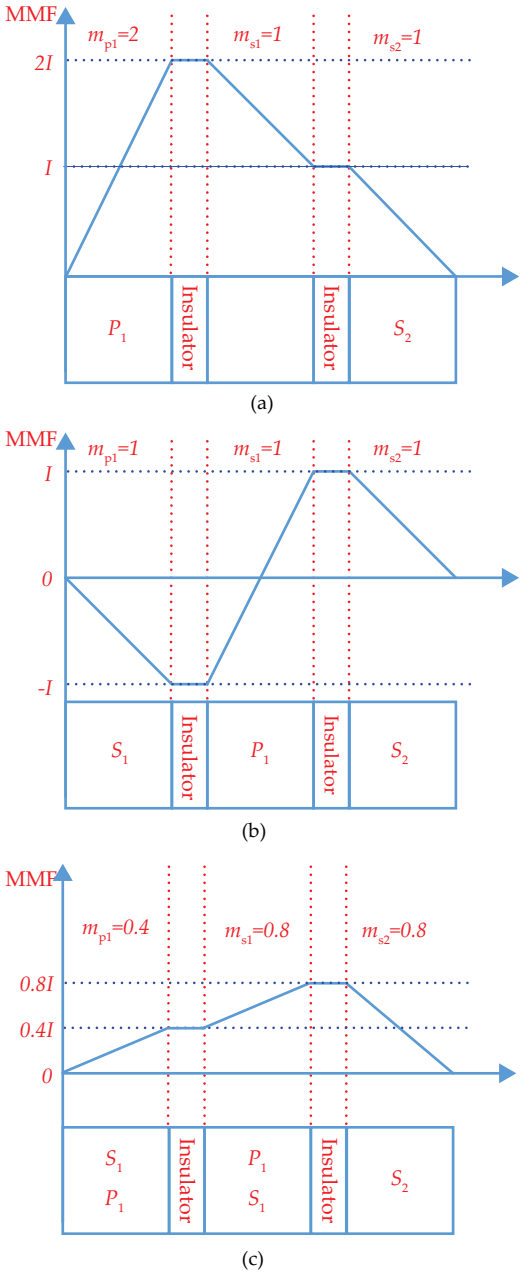


Fig. 4.6: Magnetomotive force (MMF) distribution based on different winding configurations: (a) W_1 , (b) W_2 , and (c) W_3 [C3], [95].

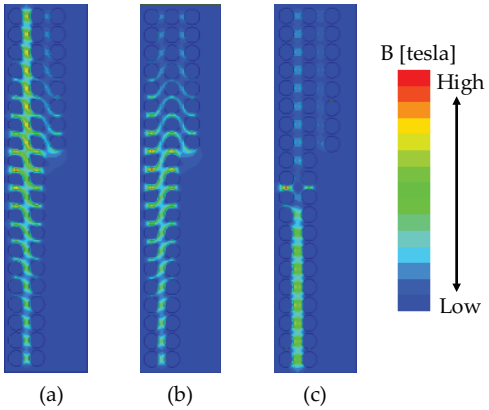


Fig. 4.7: Simulation results of the energy in the inductor: (a) non-interleaved(P/S), (b) partially interleaved (S/P/S), and (c) fully-interleaved (PS/SP/S) [C3], [95].

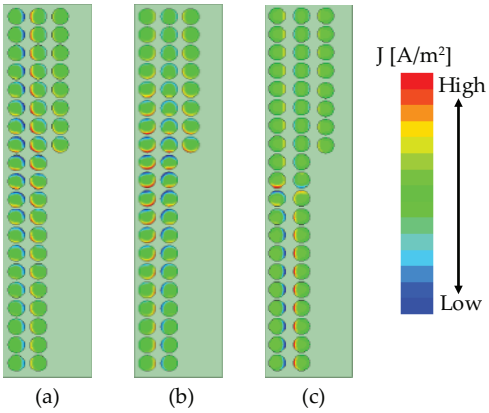


Fig. 4.8: Simulation results of the AC current density in the inductor: (a) non-interleaved(P/S), (b) partially interleaved (S/P/S), and (c) fully-interleaved (PS/SP/S) [C3], [95].

Table 4.3 presents the parameters of the leakage inductance and AC resistance for windings W_1, W_2 and W_3. The simulation and measured results roughly conform to the previous FEM analysis, where the interleaved structure could provide lower parasitics. Moreover, the winding W_3 has the lowest parasitics compared to the other windings because of its more interleaved structure.

Fig. 4.9 shows the experimental results by using W_1,W_2 and W_3. Under the same experimental condition, it is noticeable in Fig. 4.9 that the output voltages in these three winding structures are 366 V, 385 V, and 395 V, respectively [C3], [95]. Therefore, the performance of the winding structure W_3 is better than the other two structures due to low parasitics. Furthermore, by comparing the waveforms of the diode voltage V_{D2}, it is clear that the diode voltage in the winding W_3 is not affected due to its extremely small leakage inductance. That is, the small leakage inductance can mitigate the effect of the leakage inductance in such layouts.

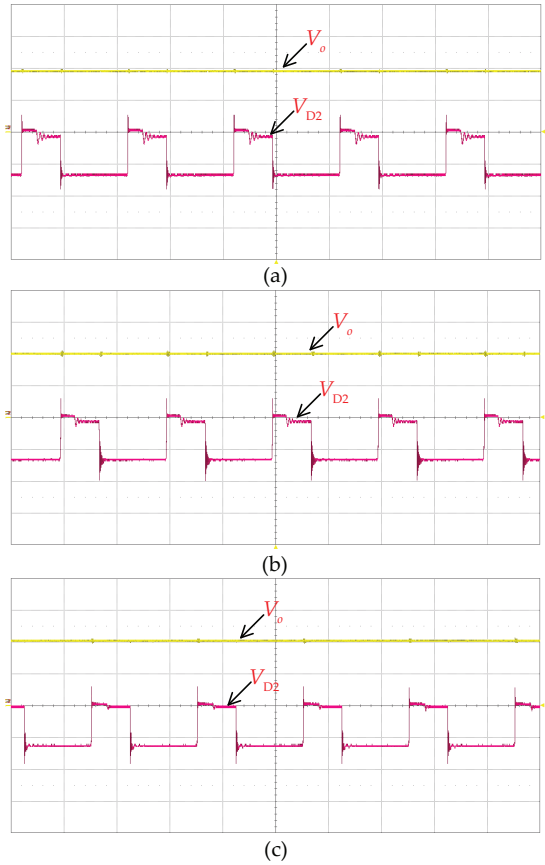


Fig. 4.9: Experimental results with different coupled inductors on the trans-inverse DC-DC converter shown in Fig. 3.2: (a) W_1 , and (b) W_2 , and (c) W_3 . (V_o (200 V/div) and V_{D2} (100 V/div)) [C3], [95].

4.5 Summary

This chapter introduces a simplified systematic design for impedance-source networks. To maximize the performance of the ISNs, several design concerns: topologies, modulation strategies, switching frequencies, and practical layout optimization are addressed. In addition, the basic design principles are provided for the capacitor and inductors. Moreover, a detailed design procedure for achieving the overall design of the ISN is demonstrated. Finally, case studies for quasi-Z-source network design and optimal design of the coupled inductors are provided.

Chapter 5

5 Conclusions and Future Work

This chapter summarizes the results and outcomes of the PhD project - *Impedance Source Converters for Renewable Energy Systems*. The main contributions are highlighted, and the research perspectives are demonstrated at the end of the chapter.

5.1 Summary

The main focus of this PhD project is on the development of novel impedance-source networks for high-efficiency and high-reliability in DC-AC and DC-DC power conversion systems. Several novel impedance-source inverters and step-up DC-DC converter topologies have been proposed. Furthermore, the design and optimization of the impedance-source networks are also explored. A summary of this PhD thesis is presented as follows.

In *Chapter 1*, the background and state-of-the-art of impedance-source networks applied in two-stage and single-stage power conversion solutions have been discussed. Thus, it is necessary to develop new impedance-source networks for high-efficiency and high reliability in the integration of renewable energy systems. And then, three research objectives are outlined: 1) development of novel impedance-source inverters; 2) improvement on the high-performance step-up DC-DC converter topologies; 3) design and optimization of the impedance-source network.

To address the limitations of the existing ZSIs, *Chapter 2* discusses several improved Z-source inverters by using non-magnetic networks. Compared with traditional ZSIs, the developed improved Z-source inverters could obtain continuous input currents, lower voltage stresses, and fault-tolerant operations, which have been validated by benchmarking studies and experimental tests.

Chapter 3 discusses modified magnetic-based impedance-source DC-DC converters. Compared to various DC-DC converters, the proposed TICSC and MYSC feature continuous input currents, trans-inverse capability, and a wide adjustable duty cycle range. In addition, the possible DC current saturation of the magnetic core is addressed by the configuration of the circuit topology. And then, benchmarking results are provided and two prototypes have been built to validate the performance of the TICSC and MYSC.

Finally, *Chapter 4* presents a simple systematic design for the impedance-source network. Topologies, modulation strategies, switching frequencies, and practical layout are considered in the design. Additionally, the design guidelines for the capacitors and inductors were performed. And then, a thorough design procedure for impedance-source networks is proposed. At last, case studies are conducted based on the above-discussed design concerns and procedures.

5.2 Contributions

The main contributions of this PhD project are summarized as follows:

A) Development of improved Z-source inverter

- An embedded enhanced-boost Z-source inverter (EEB-ZSI) and a switched quasi-Z-source inverter (S-qZSI), which features a continuous input current, high voltage gain, low voltage stresses across the components, and fault-tolerant operations were proposed;
- The operation principle analysis and benchmarking were conducted for the proposed EEB-ZSI and S-qZSI;
- The prototypes were built up, and the performance of the EEB-ZSI and S-qZSI was validated through experimental tests.

B) Modified impedance-source DC-DC converter

- Two modified impedance-source DC-DC converters (the TICSC and MYSC) based on the coupled inductors were proposed;
- The characteristics in terms of continuous input, trans-inverse capability, and a wide adjustable duty cycle range were discussed;
- Two prototypes have been built and tested for verification.

C) Design and optimization of impedance-source network

- Several design considerations for impedance-source networks, i.e., topologies, modulation strategies, and switching frequencies were explored;
- A systematic design method for the impedance-source networks was proposed and validated by a case study;
- A design optimization with different winding configurations for coupled inductors was provided.

5.3 Research Perspectives

Although this project has brought some new outcomes, there are still other new research possibilities as further work:

- New impedance-source networks in DC-AC and DC-DC power conversion systems have been introduced in this PhD project. However, the volume of the prototype is relatively large due to higher component counts. Therefore, it would be interesting to develop the impedance-source inverter by applying planar inductors and SiC/GaN devices. In addition, another promising solution based on the impedance-source network is to develop the module-integrated design, such as to integrate the impedance-source network on the PV panels.

- The research related to the impedance-source networks is widely conducted in academia. However, the impedance-source networks are rarely applied in industrial applications. A comprehensive performance benchmark between the impedance-source network and traditional converters might be attractive for industry.
- A systematic design of impedance-source networks was introduced in this PhD project. However, this design method only focuses on basic design criteria. It would be helpful to conduct multi-objective optimization considering the efficiency, power density, costs, reliability for different applications. In addition, the mission profiles should be considered in the design process for different applications.
- Regarding the possible solutions to improve the integration, this PhD project only discussed the impedance-source topologies. In fact, it can be further improved by advanced control methods. Therefore, to apply the impedance-source networks to the renewable energy systems, the impedance-source converter and the grid-connected inverter should be modeled, and then, control strategies can be designed.
- In order to improve the power density of impedance-source converters, the switching frequency of the power switch should be increased. Thus, the power switches during high-frequency operations may make electromagnetic noise, which may degrade the performance of the surrounding electrical equipment and affect the overall stability of the system. Therefore, it would be interesting to investigate the electromagnetic interference (EMI)/electromagnetic compatibility (EMC) performance in industrial-related domains.

Bibliography

References

[1] H. E. Murdock, D. Gibb, T. André, F. Appavou, A. Brown, B. Epp, B. Kondev, A. McCrone, E. Musolino, L. Ranalder *et al.*, "Renewables 2019 global status report," 2019.

[2] J. Yuan, F. Blaabjerg, Y. Yang, A. Sangwongwanich, and Y. Shen, "An overview of photovoltaic microinverters: Topology, efficiency, and reliability," in *Proc. IEEE CPE-POWERENG 2019*, 2019, pp. 1–6.

[3] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep. 2005.

[4] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.

[5] Y. Kim, S. Shin, J. Lee, Y. Jung, and C. Won, "Soft-switching current-fed push-pull converter for 250-W AC module applications," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 863–872, Feb. 2014.

[6] S. Kouro, J. I. Leon, D. Vinnikov, and L. G. Franquelo, "Grid-connected photovoltaic systems: An overview of recent research and emerging PV converter technology," *IEEE Ind. Electron. Mag.*, vol. 9, no. 1, pp. 47–61, Mar. 2015.

[7] D. Meneses, F. Blaabjerg, O. García, and J. A. Cobos, "Review and comparison of step-up transformerless topologies for photovoltaic AC-module application," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2649–2663, Jun. 2013.

[8] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 184–191, Jan. 2011.

[9] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep. 2005.

[10] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC-DC PWM converters," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 2, pp. 687–696, Mar. 2008.

[11] Y. Hu, K. Li, Z. Yin, and A. Ioinovici, "Switched-inductor-based non-isolated large conversion ratio, low components count DC-DC regulators," in *Proc. IEEE ECCE*, Sep. 2015, pp. 1398–1405.

[12] K. Li, Y. Hu, and A. Ioinovici, "Generation of the large DC gain step-up non-isolated converters in conjunction with renewable energy sources starting from a proposed geometric structure," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5323–5340, July 2017.

[13] S. Jain and V. Agarwal, "A single-stage grid connected inverter topology for solar PV systems with maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1928–1940, Sep. 2007.

[14] O. Abdel-Rahim, M. Orabi, and M. E. Ahmed, "Buck-boost interleaved inverter for grid connected photovoltaic system," in *Proc. IEEE ICPE*, Nov. 2010, pp. 63–68.

[15] G. Tan, J. Wang, R. Wang, and Y. Ji, "A new SPWM controlled three-switch buck-boost inverter for distributed generation applications," in *Proc. IEEE ICPST*, Oct. 2006, pp. 1–6.

[16] Y. Zhang, A. T. Woldegiorgis, and L. Chang, "Design and test of a novel buck-boost inverter with three switching devices," in *Proce. IEEE APEC*, Feb. 2012, pp. 1973–1978.

[17] O. Ellabban and H. Abu-Rub, "Z-source inverter: Topology improvements review," *IEEE Ind. Electron. Mag.*, vol. 10, no. 1, pp. 6–24, Mar. 2016.

[18] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar. 2003.

[19] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-source networks for electric power conversion part I: A topological review," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 699–716, Feb. 2015.

[20] Y. Liu, H. Abu-Rub, B. Ge, F. Blaabjerg, O. Ellabban, and P. C. Loh, *Impedance source power electronic converters*. John Wiley & Sons, 2016.

[21] J. Yuan, A. Mostaan, Y. Yang, Y. P. Siwakoti, and F. Blaabjerg, "Modified impedance-source inverter with continuous input currents and fault-tolerant operations," *Energies*, vol. 13, no. 13, p. 3408, Jul. 2020.

[22] S. K. Mazumder, R. K. Burra, and K. Acharya, "A ripple-mitigating and energy-efficient fuel cell power-conditioning system," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1437–1452, Jul. 2007.

[23] A. E. Khateb, N. A. Rahim, J. Selvaraj, and B. W. Williams, "The effect of input current ripple on the photovoltaic panel efficiency," in *Proc. IEEE CEAT*, 2013, pp. 478–481.

[24] Y. P. Siwakoti, F. Blaabjerg, V. P. Galigekere, A. Ayachit, and M. K. Kazimierczuk, "A-source impedance network," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8081–8087, Dec. 2016.

[25] J. Yuan, Y. Yang, P. Liu, Y. Shen, and F. Blaabjerg, "An embedded switched-capacitor Z-source inverter with continuous input currents," in *Proc. IEEE APEC 2019*, 2019, pp. 2366–2371.

[26] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *Proc. IEEE Power Electron. Sec. Conf.*, Rhodes, Jun. 2008, pp. 2743–2749.

[27] M. Zhu, K. Yu, and F. L. Luo, "Switched inductor Z-source inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2150–2158, Aug. 2010.

[28] M. K. Nguyen, Y. C. Lim, and G. B. Cho, "Switched-inductor quasi-Z-source inverter," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3183–3191, Nov. 2011.

[29] M. K. Nguyen, Y. C. Lim, and J. H. Choi, "Two switched-inductor quasi-Z-source inverters," *IET Power Electron.*, vol. 5, no. 7, pp. 1017–1025, Aug. 2012.

[30] D. Li, P. C. Loh, M. Zhu, F. Gao, and F. Blaabjerg, "Generalized multicell switched-inductor and switched-capacitor Z-source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 837–848, Feb. 2013.

[31] B. Poorali, A. Torkan, and E. Adib, "High step-up Z-source DC-DC converter with coupled inductors and switched capacitor cell," *IET Power Electron.*, vol. 8, no. 8, pp. 1394–1402, Jul. 2015.

[32] V. R. Vakacharla, M. Raghuram, and S. K. Singh, "Hybrid switched inductor impedance source converter—a decoupled approach," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7509–7521, Nov. 2016.

[33] Y. Zhang, C. Fu, M. Sumner, and P. Wang, "A wide input-voltage range quasi-Z-source boost DC-DC converter with high-voltage gain for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5201–5212, Jun. 2018.

[34] Y. Wang, Q. Bian, X. Hu, Y. Guan, and D. Xu, "A high-performance impedance-source converter with switched inductor," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3384–3396, Apr. 2019.

[35] S. Rostami, V. Abbasi, and F. Blaabjerg, "Implementation of a common grounded Z-source DC-DC converter with improved operation factors," *IET Power Electron.*, vol. 12, no. 9, pp. 2245–2255, Aug. 2019.

[36] S. Rostami, V. Abbasi, and T. Kerekes, "Switched capacitor based Z-source DC-DC converter," *IET Power Electron.*, vol. 12, no. 13, pp. 3582–3589, Nov. 2019.

[37] C. J. Gajanayake, F. L. Luo, H. B. Gooi, P. L. So, and L. K. Siow, "Extended-boost Z-source inverters," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2642–2652, Oct. 2010.

[38] A. Ravindranath, S. K. Mishra, and A. Joshi, "Analysis and PWM control of switched boost inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5593–5602, Dec. 2013.

[39] M. Nguyen, T. Le, S. Park, and Y. Lim, "A class of quasi-switched boost inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1526–1536, Mar. 2015.

[40] A. Ho, T. Chun, and H. Kim, "Extended boost active-switched-capacitor/switched-inductor quasi-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5681–5690, Oct. 2015.

[41] X. Zhu and B. Zhang, "High step-up quasi-Z-source DC-DC converters with single switched capacitor branch," *J. Mod Power Syst. Clean Energy*, vol. 5, no. 4, pp. 537–547, Jul. 2017.

[42] M. Hasan Babayi Nozadian, E. Babaei, S. H. Hosseini, and E. Shokati Asl, "Steady-state analysis and design considerations of high voltage gain switched Z-source inverter with continuous input current," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5342–5350, Jul. 2017.

[43] Y. Zhang, Q. Liu, J. Li, and M. Sumner, "A common ground switched-quasi-Z-source bidirectional DC-DC converter with wide-voltage-gain range for EVs with hybrid energy sources," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5188–5200, Jun. 2018.

[44] A. Ahmad, V. K. Bussa, R. K. Singh, and R. Mahanty, "Switched-boost-modified Z-source inverter topologies with improved voltage gain capability," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 4, pp. 2227–2244, Dec. 2018.

[45] Y. Zhang, Q. Liu, Y. Gao, J. Li, and M. Sumner, "Hybrid switched-capacitor/switched-quasi-Z-source bidirectional DC-DC converter with a wide voltage gain range for hybrid energy sources evs," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2680–2690, Apr. 2019.

[46] J. Liu, J. Wu, J. Qiu, and J. Zeng, "Switched Z-source/quasi-Z-source DC-DC converters with reduced passive components for photovoltaic systems," *IEEE Access*, vol. 7, pp. 40 893–40 903, Mar. 2019.

[47] A. Ahmad, R. K. Singh, and A. R. Beig, "Switched-capacitor based modified extended high gain switched boost Z-source inverters," *IEEE Access*, vol. 7, pp. 179 918–179 928, Dec. 2019.

[48] P. Kumar and M. Veerachary, "Z-network plus switched-capacitor boost DC-DC converters," *IEEE J. Emerg. Sel. Top. Power Electron.*, pp. 1–1, 2019, doi: 10.1109/JESTPE.2019.2959078.

[49] R. Majeed and A. H. Chughtai, "Multi-cell schemes for active-switched-capacitor and active-switched-capacitor/switched-inductor quasi Z-source inverters," *IEEE J. Emerg. Sel. Top. Power Electron.*, pp. 1739–1754, Feb. 2020.

[50] M. M. Haji-Esmaeili, E. Babaei, and M. Sabahi, "High step-up quasi-Z-source DC-DC converter," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10 563–10 571, Dec. 2018.

[51] P. C. Loh, F. Gao, and F. Blaabjerg, "Embedded EZ-source inverters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 1, pp. 256–267, Jan. 2010.

[52] F. Gao, P. C. Loh, D. Li, and F. Blaabjerg, "Asymmetrical and symmetrical embedded Z-source inverters," *IET Power Electron.*, vol. 4, no. 2, pp. 181–193, Feb. 2011.

[53] E. Babaei, E. Shokati Asl, M. Hasan Babayi, and S. Laali, "Developed embedded switched-Z-source inverter," *IET Power Electron.*, vol. 9, no. 9, pp. 1828–1841, Jul. 2016.

[54] M. Abbasi, A. H. Eslahchi, and M. Mardaneh, "Two symmetric extended-boost embedded switched-inductor quasi-Z-source inverter with reduced ripple continuous input current," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5096–5104, Jun. 2018.

[55] S. Khani, L. Mohammadian, S. H. Hosseini, and K. R. Milani, "Application of embedded Z-source inverters in grid connected photovoltaic systems," in *Proc. Elect. Power Distri. Con.*, Apr. 2013, pp. 1–5.

[56] K. Shiluveru, A. Singh, A. Ahmad, R. K. Singh, and A. R. Beig, "Switched capacitor embedded high gain impedance source DC-DC converter," in *Proc. IEEE IECON*, vol. 1, Oct. 2019, pp. 5045–5050.

[57] C. A. Munjaji and A. V. Tamhane, "An embedded-Z (EZ) source inverter feed based industrial adjustable speed drive system," in *Proc. IEEE ICEEOT*, Mar. 2016, pp. 966–971.

[58] A. Ho, A. Huynh, and T. Chun, "Switched-capacitor embedded quasi-DC-source inverters with advanced boosting capability," in *Proc. IEEE ICIT*, Feb. 2019, pp. 1093–1098.

[59] A. Ho, Ji-Suk Hyun, T. Chun, and H. Lee, "Embedded quasi-DC-source inverters based on active switched-capacitor structure," in *Proc. IEEE IECON*, Oct. 2016, pp. 3384–3389.

[60] A. Ho and T. Chun, "A single-phase symmetrical embedded modified-quasi-DC-source hybrid three-level inverter," in *Proc. IEEE PEMC*, Aug. 2018, pp. 962–967.

[61] R. Strzelecki, M. Adamowicz, N. Strzelecka, and W. Bury, "New type T-source inverter," in *Proc. IEEE CPE*, May 2009, pp. 191–195.

[62] W. Qian, F. Z. Peng, and H. Cha, "Trans-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3453–3463, Dec. 2011.

[63] D. Li, P. C. Loh, M. Zhu, F. Gao, and F. Blaabjerg, "Cascaded multicell trans-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 826–836, Feb. 2013.

[64] M. Nguyen, Y. Lim, and S. Park, "Improved trans-Z-source inverter with continuous input current and boost inversion capability," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4500–4510, Oct. 2013.

[65] P. C. Loh, D. Li, and F. Blaabjerg, "Γ-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4880–4884, Nov. 2013.

[66] W. Mo, P. C. Loh, and F. Blaabjerg, "Asymmetrical Γ-source inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 637–647, Feb. 2014.

[67] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, and G. E. Town, "Y-source impedance network," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3250–3254, Jul. 2014.

[68] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "Quasi-Y-source boost DC–DC converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6514–6519, Dec. 2015.

[69] Z. Aleem and M. Hanif, "Operational analysis of improved Γ-Z-source inverter with clamping diode and its comparative evaluation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 12, pp. 9191–9200, Dec. 2017.

[70] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, and G. E. Town, "Effects of leakage inductances on magnetically coupled Y-source network," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5662–5666, Nov. 2014.

[71] Y. Wang, W. Jing, Y. Qiu, Y. Wang, X. Deng, K. Hua, B. Hu, and D. Xu, "A family of Y-source DC/DC converter based on switched inductor," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1587–1597, Mar. 2019.

[72] A. Hakemi, M. Sanatkar-Chayjani, and M. Monfared, "Δ-source impedance network," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 7842–7851, Oct. 2017.

[73] H. Fathi and H. Madadi, "Enhanced-boost Z-source inverters with switched Z-impedance," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 691–703, Feb. 2016.

[74] A. Ho, S. Yang, T. Chun, and H. Lee, "Topology of modified switched-capacitor Z-source inverters with improved boost capability," in *Proc. IEEE APEC*, Mar. 2017, pp. 685–689.

[75] V. F. Pires, A. Cordeiro, D. Foito, and J. F. Martins, "Quasi-Z-source inverter with a T-type converter in normal and failure mode," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7462–7470, Nov. 2016.

[76] V. F. Pires, D. Foito, and A. Cordeiro, "Three-phase qZ-source inverter with fault tolerant capability," *IET Power Electron.*, vol. 10, no. 14, pp. 1852–1858, Nov. 2017.

[77] M. R. A and K. Sivakumar, "A fault-tolerant single-phase five-level inverter for grid-independent PV systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7569–7577, Dec. 2015.

[78] H. Fathi and H. Madadi, "Enhanced-boost Z-source inverters with switched Z-impedance," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 691–703, Feb. 2016.

[79] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, and D. J. Adams, "Constant boost control of the Z-source inverter to minimize current ripple and voltage stress," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 770–778, May 2006.

[80] J. Yuan, Y. Yang, and F. Blaabjerg, "A switched quasi-Z-source inverter with continuous input currents," *Energies*, vol. 13, no. 6, p. 1390, Mar. 2020.

[81] F. A. A. Meinagh, J. Yuan, and Y. Yang, "Analysis and design of a high voltage gain quasi-Z-source DC-DC converter," *IET Power Electronics*, vol. 2, no. 6, pp. 665–674, Feb. 2020.

[82] A. Mostaan, J. Yuan, Y. P. Siwakoti, S. Esmaeili, and F. Blaabjerg, "A trans-inverse coupled-inductor semi-SEPIC DC/DC converter with full control range," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10 398–10 402, Nov. 2019.

[83] J. Yuan, A. Mostaan, Y. Yang, Y. P. Siwakoti, and F. Blaabjerg, "A modified Y-source DC–DC converter with high voltage-gains and low switch stresses," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7716–7720, Aug. 2020.

[84] Y. P. Siwakoti, F. Blaabjerg, and P. Chiang Loh, "High step-up trans-inverse (Tx^{-1}) DC-DC converter for the distributed generation system," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4278–4291, Jul. 2016.

[85] H. Liu, J. Wang, and Y. Ji, "A novel high step-up coupled-inductor DC-DC converter with reduced power device voltage stress," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 3, pp. 1941–1948, Sep. 2019.

[86] H. Liu, F. Li, and P. Wheeler, "A family of DC-DC converters deduced from impedance source DC-DC converters for high step-up conversion," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6856–6866, Nov. 2016.

[87] L. Schmitz, R. F. Coelho, and D. C. Martins, "High step-up high efficiency DC-DC converter for module-integrated photovoltaic applications," in *Proc. 2015 COBEP/SPEC*, Nov. 2015, pp. 1–6.

[88] R. Moradpour, H. Ardi, and A. Tavakoli, "Design and implementation of a new SEPIC-based high step-up DC/DC converter for renewable energy applications," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1290–1297, Feb. 2018.

[89] Y. Tang, D. Fu, T. Wang, and Z. Xu, "Hybrid switched-inductor converters for high step-up conversion," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1480–1490, Mar. 2015.

[90] J. Yuan, Y. Yang, and F. Blaabjerg, "Systematic design of impedance source inverters," in *Proc. IEEE COMPEL 2020*, 2020, under review.

[91] Y. Zhou, L. Liu, and H. Li, "A high-performance photovoltaic module-integrated converter (MIC) based on cascaded quasi-Z-source inverters (qZSI) using eGaN FETs," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2727–2738, Jun. 2013.

[92] F. Z. Peng, M. Shen, and Z.Qian, "Maximum boost control of the Z-source inverter," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 833–838, Jul. 2005.

[93] M. Shen, Jin Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, and D. J. Adams, "Maximum constant boost control of the Z-source inverter," in *Proc. IAS Annual Metting*, vol. 1, 2004, p. 147.

[94] M. Shen, A. Joseph, Y. Huang, F. Z. Peng, and Z. Qian, "Design and development of a 50kW Z-source inverter for fuel cell vehicles," in *Proc. CES/IEEE IPEMCC*, vol. 2, Aug. 2006, pp. 1–5.

[95] J. Yuan, Z. Shen, Y. Yang, A. Mostaan, and F. Blaabjerg, "Design and analysis of a novel trans-inverse DC-DC converter," in *Proc. IEEE COMPEL 2019*, 2019, pp. 1–5.

[96] L. Liu, H. Li, Y. Zhao, X. He, and Z. J. Shen, "1 MHz cascaded Z-source inverters for scalable grid-interactive photovoltaic (PV) applications using GaN device," in *Proc. IEEE ECCE*, Sep. 2011, pp. 2738–2745.

[97] H. Cha, Y. Li, and F. Zheng Peng, "Practical layouts and DC-rail voltage clamping techniques of Z-source inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7471–7479, Nov. 2016.

[98] Y. Li, J. Anderson, F. Z. Peng, and D. Liu, "Quasi-Z-source inverter for photovoltaic power generation systems," in *Proc. IEEE APEC*, Feb. 2009, pp. 918–924.

Selected Publications

Journal publication 1

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Modified Impedance-Source Inverter with Continuous Input Currents and Fault-Tolerant Operations

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Abstract: Impedance-source (Z-source) inverters are increasingly adopted in practice, where a high voltage gain is required. However, issues like drawing a non-continuous current from the DC source and ceasing the energy supply under DC source faults are also observed. In this paper, an embedded enhanced-boost Z-source inverter (EEB-ZSI) is thus proposed to tackle the issues. The proposed EEB-ZSI employs two DC sources, which enable the continuous input current and fault-tolerant operations (e.g., open-circuit and short-circuit faults in the DC sources). The operational principles are presented in detail with an in-depth circuit analysis. Moreover, the proposed EEB-ZSI is benchmarked with prior-art Z-source inverters. Experimental tests further demonstrate the effectiveness of EEB-ZSI regarding the continuous input current and flexible fault tolerance.

Keywords: impedance source converter; Z-source inverter; switched-inductor; fault-tolerant; continuous input current

1. Introduction

Impedance source (Z-source) inverters are becoming promising in industrial applications, e.g., photovoltaic and fuel cell systems, because of their superior performance [1–7]. Conventionally, voltage source inverters (VSI) can only operate in buck operation. To address this issue, Z-source inverters, e.g., the Z-source inverter (ZSI) [8], with a larger boost ratio were introduced in the literature. Notably, a shoot-through state is added into the traditional modulation algorithm. In addition, the application of impedance-source inverters reduces the overall system cost and improves the efficiency as a single-stage power conversion solution to some extent [7]. Nevertheless, ZSIs have certain drawbacks. For example, they may draw a discontinuous input current, attain a large voltage stress across the component, and result in a poor power quality [9]. These hinder the applications of ZSI systems to some extent. Hence, tremendous efforts have been made in the literature to improve the performance and applicability of ZSI, generally through topological innovations and advanced modulation algorithms. As a representative topology among the prior-art ZSIs, the quasi Z-source inverter (qZSI) provides an effective solution to the above drawbacks [10]. Thus, many explorations of the qZSI have been presented in the literature in terms of modulation strategies to improve the efficiency and reliability.

At the same time, a vast array of impedance-source networks has been introduced to further improve the boosting capability, while also addressing the above limitations. Clearly, increasing the voltage gain could be attained by applying more passive components or active switches to the basic Z-source network, as indicated in Figure 1a. With this principle, switched-inductor (SI) or switched-capacitor (SC) cells can be used to replace the inductors or capacitors in the original ZSI or qZSI, thus leading to a higher boost ratio [11,12]. For instance, SI cells are placed in the qZSI to ensure continuous input current and low voltage stress [13]. Nevertheless, more passive components makes the inverter volume much larger compared to the basic Z-source inverter.

Additionally, the voltage gain can be increased by cascading the impedance-source networks. To achieve superior performance in terms of boosting capability and low voltage stresses across the components, the extended-boosted ZSI topologies were proposed in [14,15]. In addition, from [16], several enhanced-boost ZSIs (EB-ZSI) in Figure 1b are presented, and an enhanced boosting capability can be achieved in contrast to the topologies in [14,15]. However, the major drawbacks of these topologies are discontinuous input current and large starting inrush current. It should be noted that the performance of renewable energy systems is closely related to the input current waveform. In a fuel cell system, high ripple input current might lead to an increment of the fuel consumption, so the overall efficiency is degraded [17]. Moreover, the converters with continuous input currents are more promising in PV systems considering the accuracy of the maximum power point tracking (MPPT) [18]. Therefore, the converters with continuous input currents are welcome to be applied in the low voltage scenario to suppress the stress and improve the lifetime of the voltage source. Accordingly, a modified qZSI inverter with two switched impedance networks was introduced in [19]. This topology features a continuous input current and lower voltage stresses over the components due to its common ground between the source and bridge.

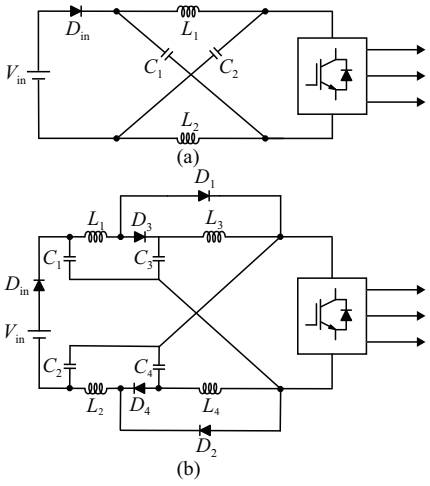

Figure 1. Two impedance networks feeding a conventional two level three phase inverter: (**a**) Z-source network [8] and (**b**) enhanced-boost Z-source network [16]. Here, V_{in} is the input voltage, and D, C, and L with subscripts represent diodes, capacitors, and inductors in the impedance network.

Furthermore, the DC current of the ZSI is normally chopped due to the existence of the diodes, as observed in Figure 1a. To address this, embedded Z-source inverters were proposed [20–22], as exemplified in Figure 2. It can be seen in Figure 2 that an embedded ZSI (E-ZSI) has two DC sources, which are directly connected in series with the inductors of the conventional ZSI shown in Figure 1a. In [22], the embedded sources were further developed into the asymmetrical and

symmetrical structures depending on the embedded source position, which can achieve implicit source current or voltage filtering without extra hardware. Although the above embedded ZSIs can overcome certain drawbacks, which exist in the conventional Z-source inverter, no significant improvement can be achieved regarding the boost capability.

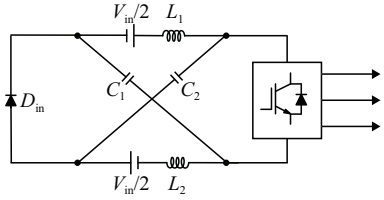

Figure 2. Example of an embedded Z-source inverter, where two identical DC sources are connected in series with the inductors of the Z-source network shown in Figure 1a [20].

Beyond topological and modulation improvements, the fault-tolerant capability is of high concern in practical applications to ensure the security of power supply. The prior-art impedance source topologies with fault-tolerance capabilities were only paying attention to power switch failures. For example, Ref. [23] introduced a topology that includes two symmetrical quasi-Z-source networks and a T-type inverter. Then, the modified modulation scheme can be used to achieve the fault-tolerance operations without applying additional phase legs to the main topology. In addition, Ref. [24] introduced a modified topology, which can operate in the abnormal conditions by using two legs. However, apart from switch failures, DC source failures may also occur practically, leading to system shutdown and interrupted power supply. For instance, in PV applications, the two DC sources may produce different currents due to shading [25]. Even for single-source impedance-source networks, low DC voltage or open-circuit faults may happen. However, the above topologies have to cease energizing the load in these cases. Thus, to ensure secure power supply, continuous input current, and also high boost gain, advanced impedance-source networks should be developed for PV applications.

In light of all the previous limitations, this paper introduces a topology with continuous input current and fault-tolerance capabilities, while maintaining a high boosting ratio. The proposed embedded enhanced-boost Z-source inverter (EEB-ZSI) is based on the embedded Z-source and switched impedance-source networks. Consequently, the proposed EEB-ZSI not only inherits the superior high boost capability of the switched impedance inverters, but also achieves continuous input current and lower voltage stress of the capacitors. Moreover, it is revealed in this paper that the proposed EEB-ZSI can maintain a normal operation even if the DC sources are in abnormal conditions. The rest of the paper is organized as follows. The operation principle, the comparison in terms of boosting capability and voltage stress on switches and capacitors, among various topologies, and the parameter design of EEB-ZSI are presented in Section 2. The fault-tolerant operation is then analysed in detail in Section 3. Section 4 provides the experimental results to validate the effectiveness of the theoretical analysis. Finally, the concluding remarks are presented in Section 5.

2. Proposed Embedded Enhanced-Boost Z-Source Inverter

As indicated in Figure 3a, EEB-ZSI has two DC sources, which are inserted into the impedance-source network. In this section, the operation principle, the comparison of the boost capability, the voltage stresses, and the design considerations are presented.

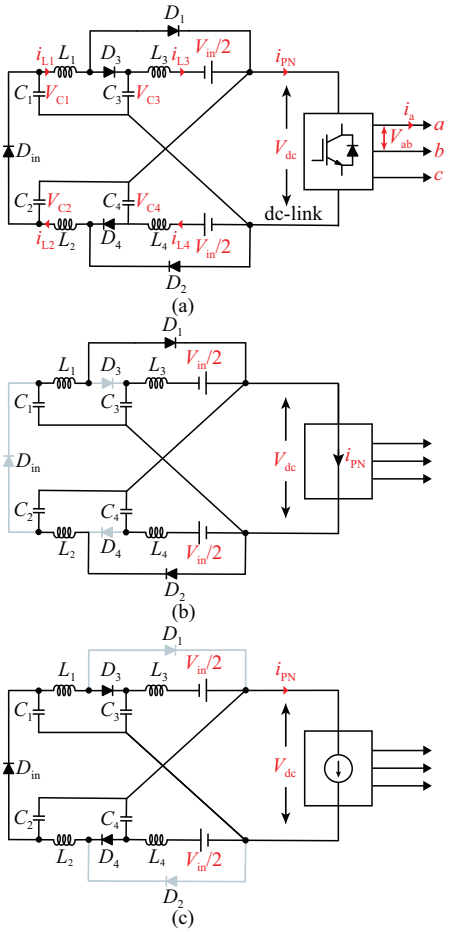

Figure 3. Proposed embedded enhanced-boost Z-source inverter (EEB-ZSI) topology: (**a**) entire circuit diagram, (**b**) equivalent circuit during the shoot-through state, and (**c**) equivalent circuit during the non-shoot-through state.

2.1. Operation Principle

As observed in Figure 3a, two switched Z-source networks are arranged in a symmetrical way, and there are two input voltage sources in the proposed EEB-ZSI.

All the inductors are defined as L_1, L_2, L_3, and L_4; all the capacitors are expressed as C_1, C_2, C_3, and C_4; all the diodes are denoted as D_1, D_2, D_3, D_4, and D_{in}.

Similar to the basic ZSI, the operation principle of EEB-ZSI can be classified into two states—the shoot-through (ST) state and the non-shoot-through (NST) state. The equivalent circuits of EEB-ZSI in the ST state and NST state are presented in Figure 3b,c, respectively. The same components in EEB-ZSI are presumed to be the same parameters. Furthermore, the input DC source voltage in EEB-ZSI is identical to the voltage being $V_{in}/2$. According to the topological symmetry, it can be obtained that

$$V_{C1} = V_{C2} \tag{1}$$

$$V_{C3} = V_{C4} \tag{2}$$

$$i_{L1} = i_{L2} \tag{3}$$

$$i_{L3} = i_{L4} \tag{4}$$

in which V_{C1}, V_{C2}, V_{C3}, and V_{C4} are the corresponding voltages across the capacitors C_1, C_2, C_3, and C_4 and i_{L1}, i_{L2}, i_{L3}, and i_{L4} are the corresponding currents flowing through the inductors L_1, L_2, L_3, and L_4. According to the previous analysis, there are two operation states:

ST State: In this case, Figure 3b shows that the DC side of the inverter is short-circuited by turning on the switches in each inverter leg simultaneously. D_1 and D_2 are the ON-state with D_3, D_4, and D_{in} being reverse-biased during the ST state. The inductors are charged by the capacitors, and no power is delivered to the AC side (the load). Then, it can be obtained that:

$$V_{C1} = V_{L1} = V_{C2} = V_{L2} \tag{5}$$

where V_{L1} and V_{L2} are the voltage of the inductor L_1 and L_2 in the ST state. Based on Kirchoff's voltage law (KVL), the inductor voltages V_{L3} and V_{L4} can be expressed as:

$$V_{L3} = V_{C3} + \frac{V_{in}}{2} \tag{6}$$

$$V_{L4} = V_{C4} + \frac{V_{in}}{2} \tag{7}$$

According to the volt-second balance principle, they can be derived:

$$DV_{L1} + (1 - D)\, V_{L1\text{-NST}} = 0 \tag{8}$$

$$DV_{L2} + (1 - D)\, V_{L2\text{-NST}} = 0 \tag{9}$$

$$DV_{L3} + (1 - D)\, V_{L3\text{-NST}} = 0 \tag{10}$$

where $V_{L1\text{-NST}}$, $V_{L2\text{-NST}}$, and $V_{L3\text{-NST}}$ are the inductor voltages on L_1, L_2, and L_3, respectively, during the NST state and D is the duty cycle. According to Equations (5)–(10), it can be derived that:

$$V_{L1\text{-NST}} = -\frac{D}{1 - D} V_{C_1} \tag{11}$$

$$V_{L2\text{-NST}} = -\frac{D}{1 - D} V_{C2} \tag{12}$$

$$V_{L3\text{-NST}} = -\frac{D}{1 - D} (V_{C3} + \frac{V_{in}}{2}) \tag{13}$$

NST State: It can be observed from Figure 3c that D_3, D_4, and D_{in} are the ON-state and D_1 and D_2 are the OFF-state. During this state, the capacitors are charged, and the load is supplied through the inverter. In addition, based on Figure 3c, the following equations can be derived by applying KVL:

$$V_{L1\text{-NST}} + V_{C3} - V_{C1} = 0 \tag{14}$$

$$V_{L1\text{-NST}} + V_{L3\text{-NST}} - \frac{V_{in}}{2} + V_{C2} = 0 \tag{15}$$

$$V_{L1\text{-NST}} - \frac{V_{in}}{2} + V_{DC}^{p} - V_{C3} = 0 \tag{16}$$

where V_{DC}^{p} is the peak DC-link voltage. Substituting (11) into (14), then it can be obtained that:

$$V_{C1} = (1 - D) V_{C3} \tag{17}$$

Then, the capacitor voltage V_{C3} and the peak DC-link voltage V_{DC}^{P} can be given as:

$$V_{C3} = \frac{1}{2D^2 - 4D + 1} \cdot \frac{V_{in}}{2} \tag{18}$$

$$V_{DC}^{P} = \frac{1 - D}{2D^2 - 4D + 1} \cdot V_{in} = B \cdot V_{in} \tag{19}$$

where:

$$B = \frac{1 - D}{2D^2 - 4D + 1} \tag{20}$$

is the boost factor. Therefore, the average DC-link voltage V_{DC} of the inverter can be expressed as:

$$V_{DC} = \frac{(1 - D)^2}{2D^2 - 4D + 1} \cdot V_{in} \tag{21}$$

The peak of the inverter output voltage V_{AC}^{P} can be given as:

$$V_{AC}^{P} = \frac{MV_{DC}^{P}}{2} = \frac{MBV_{in}}{2} = \frac{GV_{in}}{2} \tag{22}$$

in which G is the buck-boost factor and M is the modulation index. Then, the buck-boost factor can be obtained in regards to M as:

$$G = MB = \frac{M^2}{2M^2 - 1} \tag{23}$$

Following the above analysis, the relationship between the inductor currents and the peak DC-link current i_{PN} can be obtained as:

$$i_{L1} = i_{L2} = \frac{1 - D}{2D^2 - 4D + 1} \cdot i_{PN} \tag{24}$$

$$i_{L3} = i_{L4} = \frac{(1 - D)^2}{2D^2 - 4D + 1} \cdot i_{PN} \tag{25}$$

2.2. Boost Capability Comparison

Figure 4a presents the relationship of the boost factor versus the ST duty ratio among conventional ZSI [8], embedded-ZSI (E-ZSI) [20], diode-assisted ZSI (DA-ZSI) [15], switched-inductor ZSI (SI-ZSI) [11], EB-ZSI [16], and EEB-ZSI. This can be observed in Figure 4a, where the boost factor of EEB-ZSI is much larger than the other selected ZSIs owing to the extra inductors except EB-ZSI. Moreover, Figure 4b presents the relationship between the voltage gains of the selected topologies and the modulation index. The voltage gain of EEB-ZSI is higher than most of the topologies in certain ranges of the modulation index. It should be pointed out that the power quality is associated with the modulation index, and better quality might be achieved with a high modulation index. Thus, to achieve the same voltage gain, EEB-ZSI and EB-ZSI can have a higher modulation index when compared with other topologies.

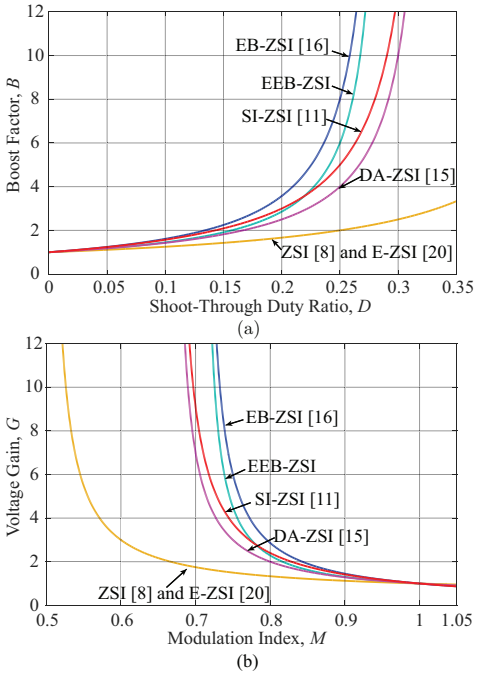

Figure 4. Comparison of the selected Z-source networks: (**a**) boost factor versus the shoot-through duty-ratio D and (**b**) voltage gain versus the modulation index M (ZSI [8], embedded-ZSI (E-ZSI) [20], diode-assisted ZSI (DA-ZSI) [15], switched-inductor ZSI (SI-ZSI) [11], and EB-ZSI [16]).

2.3. Voltage Stresses Comparison

Apart from the superior boost capability of the proposed EEB-ZSI, lower voltage stresses of EEB-ZSI are another advantage, as shown in Figure 5. The voltage stresses are specified as the proportion of the peak DC-link voltage and capacitors' voltages to the minimum DC voltage [26]. In Figure 5a, the proposed EEB-ZSI has lower voltage stresses across the switches than other selected ZSIs. Moreover, Figure 5b presents a comparison regarding the capacitor stress between EB-ZSI and EEB-ZSI. Here, the stresses across the capacitors in EEB-ZSI are lower than EB-ZSI under the same voltage gain, and thus, the performance in terms of cost and size can be improved by applying the capacitors with lower ratings. Additionally, Table 1 summarizes the benchmarking results in terms of boost factor, voltage gain, switch stress, and capacitor stresses.

Table 1. Benchmarking of selected impedance source inverters.

	Symbol	**ZSI [8]**	**E-ZSI [20]**	**DA-ZSI [15]**	**SI-ZSI [11]**	**EB-ZSI [16]**	**EEB-ZSI**
Boost Factor	B	$\frac{1}{1-2D}$	$\frac{1}{1-2D}$	$\frac{1}{1-3D}$	$\frac{1+D}{1-3D}$	$\frac{1}{2D^2-4D+1}$	$\frac{1-D}{2D^2-4D+1}$
Voltage Gain	G	$\frac{M}{2M-1}$	$\frac{M}{2M-1}$	$\frac{M}{3M-2}$	$\frac{2M-M^2}{3M-2}$	$\frac{M}{2M^2-1}$	$\frac{M^2}{2M^2-1}$
Switch Stress	$\frac{V_s}{GV_{DC}^P}$	$2-\frac{1}{G}$	$2-\frac{1}{G}$	$\frac{2G}{3G-1}$	$\frac{\sqrt{9G^2-4G+4}+2-3G}{2}$	$\frac{8G}{\left(\sqrt{8G^2+1}+1\right)^2-8G^2}$	$\frac{2G-1}{G}\sqrt{\frac{G}{2G-1}}$
C_1, C_2 Stress	$\frac{V_{C1}}{GV_{DC}^P}$, $\frac{V_{C2}}{GV_{DC}^P}$	*NA*	*NA*	*NA*	*NA*	$\frac{1+\sqrt{1+8G^2}}{4G}$	$\frac{1}{2}\sqrt{2-\frac{1}{G}}$
C_3, C_4 Stress	$\frac{V_{C3}}{GV_{DC}^P}$, $\frac{V_{C4}}{GV_{DC}^P}$	*NA*	*NA*	*NA*	*NA*	1	$1-\frac{1}{2G}$

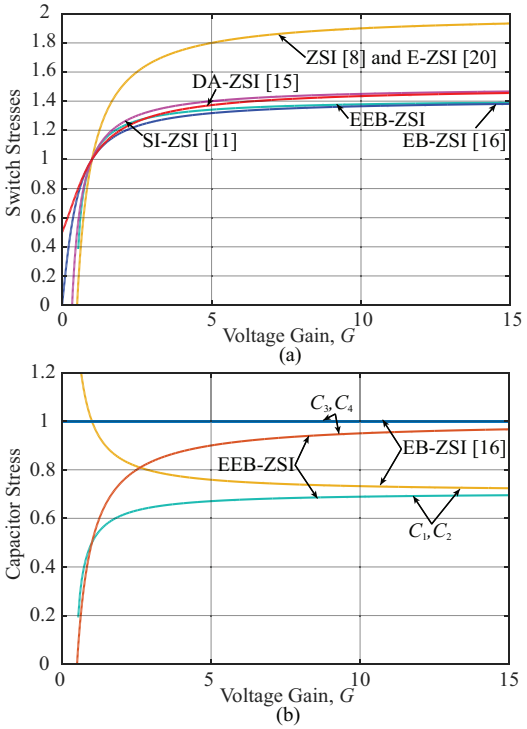

Figure 5. Comparison of the selected Z-source networks: (**a**) normalized voltage stress on the power switches and (**b**) normalized capacitor voltage stress of the EB-ZSI and the proposed EEB-ZSI.

2.4. Inductor and Capacitor Design

Based on the previous analysis, the capacitors charge the inductors, and the inductor currents increase linearly in the ST state. The inductor voltages during the ST state are presented as:

$$V_{\mathrm{L1}} = V_{\mathrm{L2}} = L\frac{di_{\mathrm{L1}}}{dt} \tag{26}$$

$$V_{\mathrm{L3}} = V_{\mathrm{L4}} = L\frac{di_{\mathrm{L3}}}{dt} \tag{27}$$

When the simple boost pulse-width modulation method is applied, there are two ST states in one switching cycle. Thus, the time interval of one ST is $DT/2$. Then, the inductors can be designed as:

$$L_1 = L_2 = \frac{D \cdot T_s}{4 \cdot \Delta i_{\mathrm{L1}}} \cdot V_{\mathrm{DC}}^{\mathrm{p}} \tag{28}$$

$$L_3 = L_4 = \frac{D\,(1-D) \cdot T_s}{2 \cdot \Delta i_{\mathrm{L3}}} \cdot V_{\mathrm{DC}}^{\mathrm{p}} \tag{29}$$

with T_s being the switching frequency and Δi_{L1} and Δi_{L3} representing the ripple currents. Similarly, the capacitors can be obtained as:

$$C_1 = C_2 = \frac{D \cdot T_s}{2 \cdot \Delta V_{\mathrm{C1}}} \cdot \frac{1-D}{2D^2 - 4D + 1} \cdot i_{\mathrm{PN}} \tag{30}$$

$$C_3 = C_4 = \frac{D \cdot T_s}{2 \cdot \Delta V_{C3}} \cdot \frac{(1-D)^2}{2D^2 - 4D + 1} \cdot i_{PN} \tag{31}$$

in which ΔV_{C1} and ΔV_{C3} are the voltage ripples for the capacitors C_1, C_2 and C_3, C_4, respectively. Notably, the ripple voltage and current on the capacitors and inductors should be determined, respectively. Subsequently, according to Equations (28)–(31), the inductors and capacitors of the proposed impedance-source network can be designed.

2.5. Control Method

To implement the proposed EEB-ZSI in the PV systems, a basic control diagram is presented in Figure 6. As discussed in [27,28], the impedance source inverters can be controlled by adjusting duty cycle D and modulation index M. More specifically, in PV systems, the duty cycle can be used to achieve the maximum power point tracking (MPPT) of the PV panel; meanwhile, the modulation index is used to control the inverter output power. As shown in Figure 6, two separate PV panels have the same input voltage V_{in} and current i_{in} assuming that they operate under the same condition. By measuring V_{in} and i_{in}, the MPPT can be achieved to generate the required voltage signal V_{in}^* [29]. Then, the duty cycle can be obtained from a proportional-integral (PI) controller. In addition, the control algorithm of the inverter side is similar to the conventional voltage source inverter. By transforming the grid/load side voltages and currents from the *abc* frame to the *dq* frame, the switching states can be determined according to the active power and reactive power closed-loop control based on the PI controllers [30].

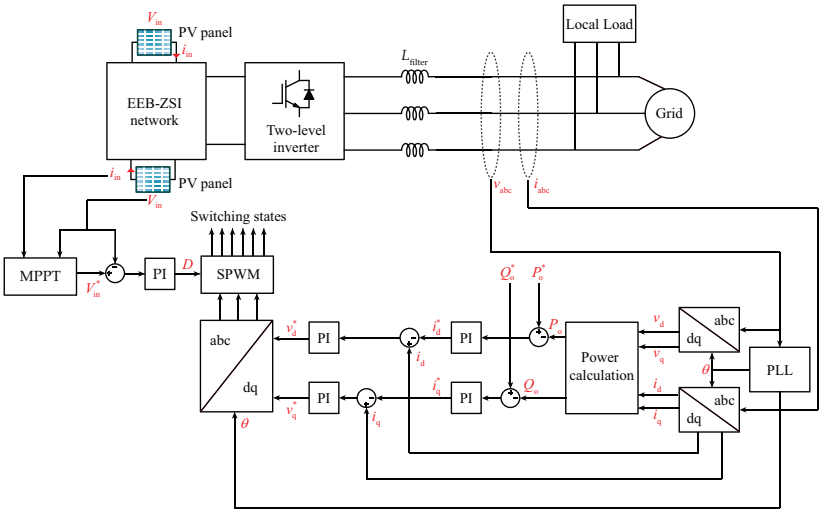

Figure 6. General control diagram for an EEB-ZSI-based PV system. (P_o, P_o^*, Q_o, and Q_o^* represent the actual/required active power and the actual/required reactive power; i_d, i_d^*, i_q, and i_q^* are the actual/required d-axis current components and the q-axis current components; v_d, v_d^*, v_q, and v_q^* are the actual/required d-axis voltage components and the q-axis voltage components; v_{abc} is the actual three-phase voltage signals; i_{abc} are the actual three-phase currents; θ is the phase angle from the phase locked loop (PLL)).

3. Fault-Tolerant Analysis

Additionally, the fault-tolerant capability of the proposed EEB-ZSI under faulty modes is another important advantage in comparison to other topologies. Detailed analysis under open-circuit (OC), short-circuit (SC), and DC source unbalance conditions is performed in this section.

3.1. Open-Circuit Analysis

Figure 7a presents the schematic of the EEB-ZSI under the OC condition, where one DC source is open-circuited. Accordingly, Figure 7b,c presents the equivalent circuits in the ST and NST states. It can be seen that C_4 and L_4 (red part) are not used for power transfer due to their disconnection from the circuit. Moreover, D_2 is in conduction mode, and D_4 is in the OFF-state during these two operation states. Then, the following equations are derived:

$$V_{DC}^{P} = \frac{1-D}{D^2-3D+1} \cdot \frac{1}{2} V_{in} \tag{32}$$

$$G = M \cdot B = \frac{M^2}{M^2+M-1}. \tag{33}$$

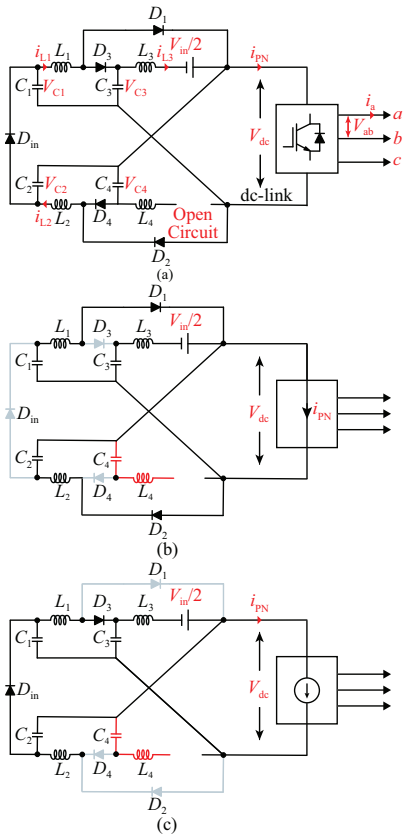

Figure 7. Circuit diagrams of the proposed EEB-ZSI under the open-circuit (a DC source) condition: (**a**) system schematic, (**b**) equivalent circuit diagram during the shoot-through state, and (**c**) equivalent circuit diagram during the non-shoot-through state.

By comparing Equations (20), (23) with (32), (33), it is clear that B and G under the OC condition are lower than those of the normal operation condition. However, the duty cycle and the modulation index can be modulated as needed to achieve the same boosting capability in both conditions.

3.2. Short-Circuit Analysis

When an SC fault happens for one DC source, EEB-ZSI can still operate, and the equivalent circuits are presented in Figure 8. In this condition, the operation is the same as that of the normal condition. However, only half of the power can be provided compared with the normal output power. Likewise, the peak DC-link voltage and voltage gain can be derived as:

$$V_{DC}^{p} = \frac{1-D}{2D^2-4D+1} \cdot \frac{1}{2} V_{in} \tag{34}$$

$$G = M \cdot B = \frac{M^2}{4M^2-2} \tag{35}$$

Assuming that the input voltages from the two DC sources are identical in normal operation, the boost capability in the SC condition is reduced by half as opposed to the normal operation.

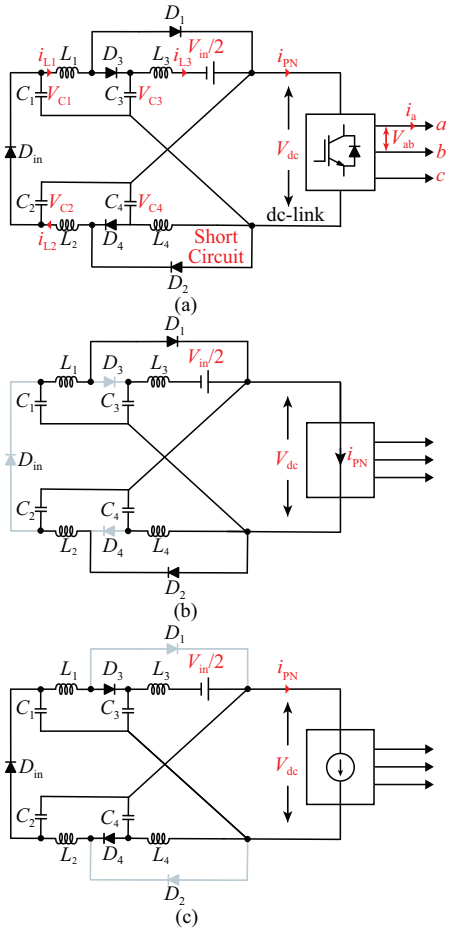

Figure 8. Circuit diagrams of the proposed EEB-ZSI under the short-circuit (a DC source) condition: (**a**) system diagram, (**b**) equivalent circuit diagram during the shoot-through state, and (**c**) equivalent circuit diagram during the non-shoot-through state.

According to the above analysis, the boost factor and voltage gain for the EEB-ZSI are further outlined in Table 2, and the corresponding relationship is shown in Figure 9. For a fair comparison, the input DC voltages are the same. In contrast to the normal operation case with the same D and M, the boosting capability of EEB-ZSI is greatly reduced due to the OC and SC faults. Nevertheless, the fault-tolerant operation can be ensured by adjusting the duty cycle and modulation index. It is noted that M should be decreased to meet the requirements of the normal condition if the faults happen, which may lead to an unexpected power quality and efficiency reduction. Therefore, this paper only discusses that the system rides through the DC faults by regulating the DC input voltage.

Table 2. Comparisons of the proposed EEB-ZSI under normal and fault conditions.

	Normal Condition	**Open-Circuit Condition**	**Short-Circuit Condition**
B	$\frac{1-D}{2D^2-4D+1}$	$\frac{1-D}{D^2-3D+1} \cdot \frac{1}{2}$	$\frac{1-D}{2D^2-4D+1} \cdot \frac{1}{2}$
$G-M$	$G=\frac{M^2}{2M^2-1}$	$G=\frac{M^2}{M^2+M-1}$	$G=\frac{M^2}{4M^2-2}$

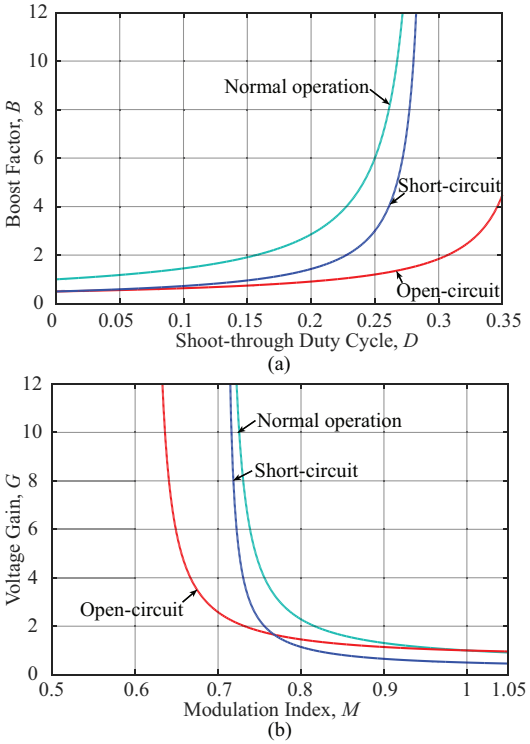

Figure 9. Comparison under normal and fault conditions: (**a**) boost factor comparison and (**b**) voltage gain comparison.

3.3. Source-Unbalance Analysis

Considering the special scenario in PV systems, the DC voltages embedded in EEB-ZSI will be different when the shaded PV modules are bypassed by diodes. In this case, the currents generated by the PV panels remain the same (identical panels). Here, the two DC sources are denoted by V_1 and

V_2. Clearly, the operation principle remains the same compared with the normal operation condition. According to the above, the peak DC-link voltage is expressed as:

$$V_{DC}^{P} = \frac{1-D}{2D^2-4D+1} \cdot (V_1 + V_2) \tag{36}$$

In contrast to Equation (19), although the equation to calculate the boost factor is not changed, the peak DC-link voltage is determined by the total voltage of the two sources. Therefore, the SC condition can be treated as a special source-unbalance case.

4. Experimental Verification

To confirm the effectiveness of EEB-ZSI under normal and faulty conditions, the prototype was built, and the experimental results are provided. The key parameters of the proposed EEB-ZSI in the experimental tests are shown in Table 3. Three cases were carried out to validate the feasibility of EEB-ZSI (i.e., normal operation and OC and SC (unbalance source) modes), and the M and D were selected as 0.85 and 0.15 in the initial state.

Table 3. Parameters of EEB-ZSI.

Parameter	Symbol	Value
DC input voltage	V_{in}	80 V
EEB-ZSI inductance	L_1, L_2, L_3, L_4	640 μH
EEB-ZSI capacitor	C_1, C_2, C_3, C_4	100 μF
Load inductance	L_f	6 mH
Load resistance	R_f	40 Ω
Switching frequency	f_s	5 kHz

Case 1: Under the normal condition, the input voltages of the proposed EEB-ZSI were the same, and the experimental results are indicated in Figure 10.

According to Equation (20), B was 1.91, and the inverter output voltage and DC-link voltage were boosted to 153 V (the peak). Figure 10 shows the experimental results for the proposed EEB-ZSI under normal operation; the DC-link voltage was boosted from 80 to 150 V. The obtained experimental result in terms of output voltage was lower than the theoretical value considering the parasitics of the components. Moreover, i_{L3} kept a continuous output state, which verified the improvement in terms of the continuous input current.

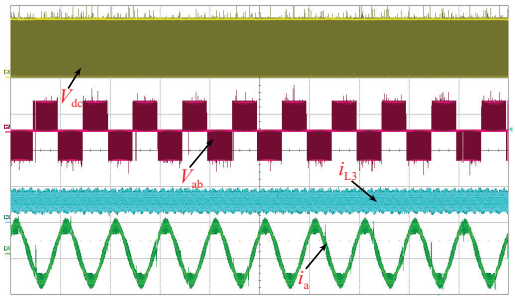

Figure 10. Experimental results of the proposed EEB-ZSI under normal operation. (V_{DC} (100 V/div), V_{ab} (200 V/div), i_{L3} (5 A/div), i_a (2 A/div), time (20 ms/div)).

Case 2: When the EEB-ZSI operated under the OC condition, the experimental results were as presented in Figure 11a. When M and D were in the initial state, the DC-link voltage was boosted to 60 V based on Equation (34), which matched with the results in Figure 11b. To further compensate

the decreased voltage under the OC condition, M and D could be adjusted to one and 0.305 based on the previous analysis. Moreover, it is clear in Figure 11a that the DC-link voltage and output voltage increased to the required value. Meanwhile, the output power increased with the increase of the input current (i_{L3}), and the load current also increased compared to the initial state.

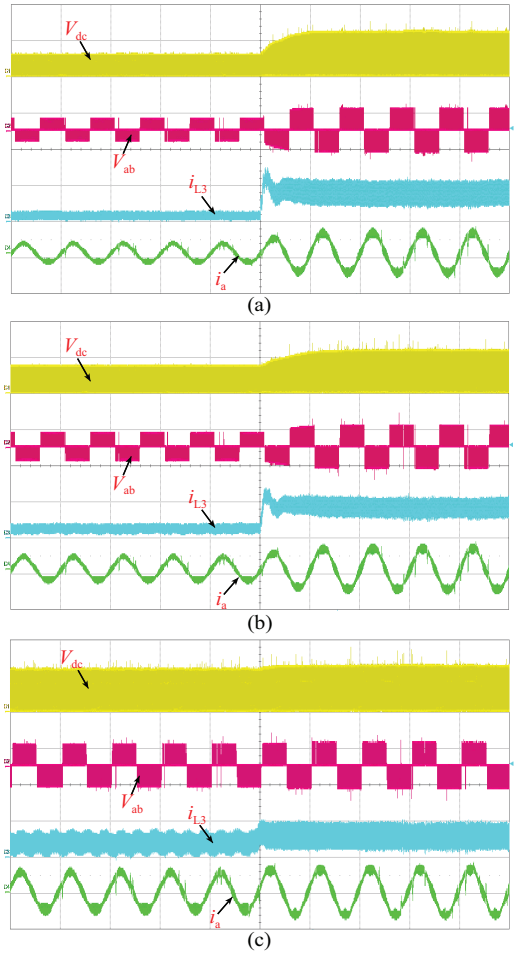

Figure 11. Experimental results of the proposed EEB-ZSI under abnormal conditions: (**a**) open-circuit (OC) condition, (**b**) short-circuit (SC) condition, and (**c**) unbalanced-source condition (V_{DC} (100 V/div), V_{ab} (200 V/div), i_{L3} (5 A/div), i_a (2 A/div), time (20 ms/div)).

Case 3: This case was carried out under the SC (unbalanced source) condition. Compared to the normal operation condition, the power was only supplied by one DC source. Therefore, the peak DC-link voltage was boosted to 75 V in the initial state, which was half of the boosted voltage in normal operation. After modulating M and D to one and 0.219, the required voltage level could be ensured, as shown in Figure 11b. In addition, in terms of unbalanced source conditions, two DC sources provided unbalanced power with two DC sources being 40 V and 20 V, respectively. According to Equation (36), the boosted voltage was calculated to be 114 V, which was three-quarters of the boosted

voltage in normal operation. Similarly, by changing M and D to one and 0.172, the boosted voltage was restored to the normal level, as shown in Figure 11c.

5. Conclusions

In this paper, an embedded enhanced-boost Z-source inverter (EEB-ZSI) with continuous input current and fault-tolerant capabilities was proposed. The operation principles were presented in detail, where the proposed topology was also compared with the prior-art solutions. Compared to the traditional embedded ZSIs and the enhanced-boost ZSI (EB-ZSI), the EEB-ZSI could realize continuous input currents, while also maintaining a high conversion ratio. Additionally, the proposed EEB-ZSI could tolerate the DC source faults with a relatively large boost ratio, where it could improve the system continuity of operation. Extensive experimental tests also confirmed the claim that the proposed EEB-ZSI was a promising impedance-source converter in terms of continuous input current, high boosting ratio, and strong fault-tolerant capability.

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References

1. Liu, Y.; Abu-Rub, H.; Ge, B.; Blaabjerg, F.; Ellabban, O.; Loh, P.C. *Impedance Source Power Electronic Converters*; John Wiley & Sons: Hoboken, NJ, USA, 2016.
2. Yang, Y.; Kim, K.A.; Blaabjerg, F.; Sangwongwanich, A. *Advances in Grid-Connected Photovoltaic Power Conversion Systems*; Woodhead Publishing: Cambridge, UK, 2018.
3. Yuan, J.; Yang, Y.; Liu, P.; Shen, Y.; Qiu, Z.; Blaabjerg, F. An embedded enhanced-boost Z-source inverter. In Proceedings of the IEEE PEAC, Shenzhen, China, 4–7 November 2018; pp. 1–6.
4. Yuan, J.; Yang, Y.; Blaabjerg, F. A switched quasi-Z-Source inverter with continuous input currents. *Energies* **2020**, *13*, 1390. [CrossRef]
5. Yuan, J.; Mostaan, A.; Yang, Y.; Siwakoti, Y.P.; Blaabjerg, F. A modified Y-Source DC/DC converter with high voltage-gains and low switch stresses. *IEEE Trans. Power Electron.* **2020**, *35*, 7716–7720. [CrossRef]
6. Mostaan, A.; Yuan, J.; Siwakoti, Y.P.; Esmaeili, S.; Blaabjerg, F. A trans-Inverse coupled-inductor semi-SEPIC DC/DC converter with full control range. *IEEE Trans. Power Electron.* **2019**, *34*, 10398–10402. [CrossRef]
7. Singh, S.A.; Carli, G.; Azeez, N.A.; Williamson, S.S. Modeling, design, control, and implementation of a modified Z-source integrated PV/Grid/EV DC charger/inverter. *IEEE Trans. Ind. Electron.* **2018**, *65*, 5213–5220. [CrossRef]
8. Peng, F.Z. Z-source inverter. *IEEE Trans. Ind. Appl.* **2003**, *39*, 504–510. [CrossRef]
9. Abdelhakim, A.; Blaabjerg, F.; Mattavelli, P. Modulation schemes of the three-phase impedance source inverters part I: Classification and review. *IEEE Trans. Ind. Electron.* **2018**, *65*, 6309–6320. [CrossRef]
10. Anderson, J.; Peng, F.Z. Four quasi-Z-Source inverters. In Proceedings of the IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008; pp. 2743–2749.
11. Zhu, M.; Yu, K.; Luo, F.L. Switched inductor Z-Source inverter. *IEEE Trans. Power Electron.* **2010**, *25*, 2150–2158.
12. Li, D.; Loh, P.C.; Zhu, M.; Gao, F.; Blaabjerg, F. Generalized multicell switched-inductor and switched-capacitor Z-Source inverters. *IEEE Trans. Power Electron.* **2013**, *28*, 837–848. [CrossRef]
13. Nguyen, M.; Lim, Y.; Cho, G. Switched-inductor quasi-Z-source inverter. *IEEE Trans. Power Electron.* **2011**, *26*, 3183–3191. [CrossRef]
14. Gajanayake, C.J.; Gooi, H.B.; Luo, F.L.; So, P.L.; Siow, L.K.; Vo, Q.N. Simple modulation and control method for new extended boost quasi Z-source. In Proceedings of the TENCON Conference, Singapore, 23–26 January 2009; pp. 1–6.

15. Gajanayake, C.J.; Luo, F.L.; Gooi, H.B.; So, P.L.; Siow, L.K. Extended-boost Z-source inverters. *IEEE Trans. Power Electron.* **2010**, *25*, 2642–2652. [CrossRef]
16. Fathi, H.; Madadi, H. Enhanced-boost Z-source inverters with switched Z-impedance. *IEEE Trans. Ind. Electron.* **2015**, *62*, 7569–7577. [CrossRef]
17. Mazumder, S.K.; Burra, R.K.; Acharya, K. A ripple-mitigating and energy-efficient fuel cell power-conditioning system. *IEEE Trans. Power Electron.* **2006**, *22*, 1437–1452. [CrossRef]
18. Khateb, A.E.; Rahim, N.A.; Selvaraj, J.; Williams, B.W. The effect of input current ripple on the photovoltaic panel efficiency. In Proceedings of the IEEE CEAT, Lankgkawi, Malaysia, 18–20 November 2013; pp. 478–481.
19. Jagan, V.; Kotturu, J.; Das, S. Enhanced-boost quasi-Z-source inverters with two-switched impedance networks. *IEEE Trans. Ind. Electron.* **2017**, *64*, 6885–6897. [CrossRef]
20. Loh, P.C.; Gao, F.; Blaabjerg, F. Embedded EZ-source inverters. *IEEE Trans. Ind. Appl.* **2010**, *46*, 256–267.
21. Babaei, E.; Asl, E.S.; Babayi, M.H.; Laali, S. Developed embedded switched-Z-source inverter. *IET Power Electron.* **2016**, *9*, 1828–1841. [CrossRef]
22. Gao, F.; Loh, P.C.; Li, D.; Blaabjerg, F. Asymmetrical and symmetrical embedded Z-source inverters. *IET Power Electron.* **2011**, *4*, 181–193. [CrossRef]
23. Pires, V.F.; Cordeiro, A.; Foito, D.; Martins, J.F. Quasi-Z-source inverter with a T-type converter in normal and failure mode. *IEEE Trans. Power Electron.* **2016**, *31*, 7462–7470. [CrossRef]
24. Pires, V.F.; Foito, D.; Cordeiro, A. Three-phase qZ-source inverter with fault tolerant capability. *IET Power Electron.* **2017**, *10*, 1852–1858. [CrossRef]
25. Sivakumar, K. A fault-tolerant single-phase five-level inverter for grid-independent PV systems. *IEEE Trans. Ind. Electron.* **2015**, *62*, 7569–7577.
26. Shen, M.; Wang, J.; Joseph, A.; Peng, F.Z.; Tolbert, L.M.; Adams, D.J. Constant boost control of the Z-source inverter to minimize current ripple and voltage stress. *IEEE Trans. Ind. Appl.* **2006**, *42*, 770–778. [CrossRef]
27. Huang, Y.; Shen, M.; Peng, F.Z.; Wang, J. Z-Source Inverter for Residential Photovoltaic Systems. *IEEE Trans. Power Electron.* **2006**, *21*, 1776–1782. [CrossRef]
28. Siwakoti, Y.P.; Peng, F.Z.; Blaabjerg, F.; Loh, P.C.; Town, G.E.; Yang, S. Impedance-Source Networks for Electric Power Conversion Part II: Review of Control and Modulation Techniques. *IEEE Trans. Power Electron.* **2015**, *30*, 1887–1906. [CrossRef]
29. Subudhi, B.; Pradhan, R. A Comparative Study on Maximum Power Point Tracking Techniques for Photovoltaic Power Systems. *IEEE Trans. Sustain. Energy* **2013**, *4*, 89–98. [CrossRef]
30. Ge, B.; Abu-Rub, H.; Peng, F.Z.; Lei, Q.; de Almeida, A.T.; Ferreira, F.J.T.E.; Sun, D.; Liu, Y. An Energy-Stored Quasi-Z-Source Inverter for Application to Photovoltaic Power System. *IEEE Trans. Ind. Electron.* **2013**, *60*, 4468–4481. [CrossRef]

Journal publication 2

A Switched-Quasi-Z-Source Inverter with Continuous Input Currents

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A Switched Quasi-Z-Source Inverter with Continuous Input Currents

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Abstract: Impedance source converters as single-stage power conversion alternatives can boost and regulate the output voltages of renewable energy sources. Nevertheless, they, also known as Z-source inverters (ZSIs), still suffer from limited voltage gains and higher stresses across the components. To tackle such issues, extra diodes, passive components, and active switches can be utilized in the basic ZSIs. In this paper, a modified switched-quasi-Z-source inverter (S-qZSI) is proposed, which features continuous input currents and high boosting capability to boost output voltage by minor modifications of a prior-art topology. Furthermore, the voltage stress of the active switches is reduced, which contributes to a lower cost. The operation principles are discussed comprehensively. The performance of the proposed ZSI in terms of conversion ratio, voltage gain, and stresses on the power switches and capacitors is benchmarked with selected ZSIs. Finally, simulations and experimental tests substantiate the theoretical analysis and superior performance.

Keywords: Z-source inverter; impedance source inverter; quasi Z-source inverter; switched boost inverter; continuous input current; DC–AC inverter

1. Introduction

Impedance source converters have gone through rapid development in the last few decades since the first Z-source inverter (ZSI) proposed by Peng in [1]. It is known that the traditional voltage source inverter (VSI) only has buck characteristics so that it is usually not directly applied in the power conversion applications. That is, a front-end stage is commonly adopted. However, the extra DC–DC converters may lead to higher costs and lower efficiency [2]. Furthermore, the power switches of the VSI may be damaged if the inverter leg is short-circuited due to wrong drive signals. To address these issues, the Z-source network, as shown in Figure 1a, which features buck-boost characteristics, can be adopted. However, the basic ZSI still suffers from certain limitations, such as discontinuous input currents and high voltage stresses across the components. The quasi-ZSI (q-ZSI), as shown in Figure 1b, provides an effective solution to the above limitations [3]. Based on the basic ZSI/qZSI structure, many attempts have been made to enhance the performance of impedance source converters in terms of high boost capability, low voltage stresses across the components, and high efficiency [4–17].

The principle of enhancing the boost capability in the impedance source networks is to add more passive components or power switches into the basic ZSI/qZSI networks. For example, the inductors in the ZSI/qZSI can be replaced by the switched-inductor (SI) cells in Figure 2, in which a higher boost voltage gain can be obtained [8–10]. Compared with the SI-ZSI, the SI-qZSI can achieve a continuous input current and lower stresses across the components. Moreover, switched-capacitor (SC) cells can be employed to obtain low voltage stress, small inductors, high voltage gains, and efficiency [11,12].

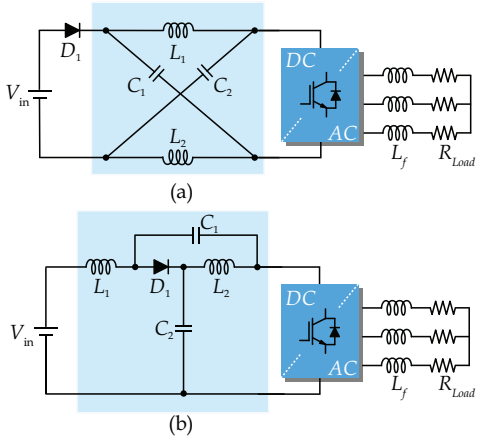

Figure 1. Circuit schematics of impedance-source-fed three-phase inverters: (**a**) Z-source inverter [1], and (**b**) quasi-Z-source inverter [3].

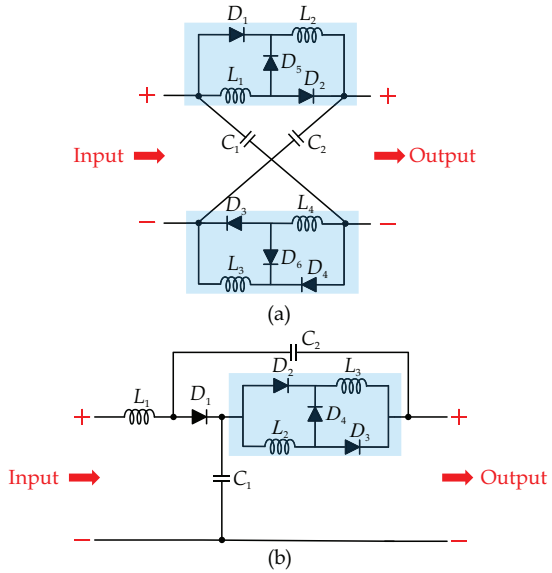

Figure 2. Modified impedance networks based on switched-inductor: (**a**) switched-inductor Z-source inverter [8], and (**b**) switched-inductor quasi-Z-source inverter [9].

Nevertheless, the limitation of these modified converters based on extra components is that many passive devices lead to a higher cost and larger volume of the converter. To tackle this, modified ZSI topologies based on switched-boost networks have been proposed in the literature. The switched-boost inverter (SBI) and embedded-qSBI are shown in Figure 3 [13,14]. The SBI features a lower number of components and the same boost capability by adding one power switch compared to the ZSI. Moreover, the q-SBI and embedded-qSBI have additional advantages, such as reduced voltage stresses on the capacitors, higher voltage gains, and continuous input currents, which makes them appropriate for renewable energy applications. Similarly, the SI or SC cells can be utilized in the SBI/qSBI for a higher

boost capability, as presented in [15]. In addition, a diode-assisted SBI (DA-SBI) was proposed in [16]. This modified topology is a combination of the SBI and diode-assisted network, which provides a high voltage gain and continuous input currents. Furthermore, the modified topology quasi-ZSI with continuous input current (CC-qZSI) in [17] shows the improved boost capabilities and less voltage stresses by adding a switched boost network to the original qZSI.

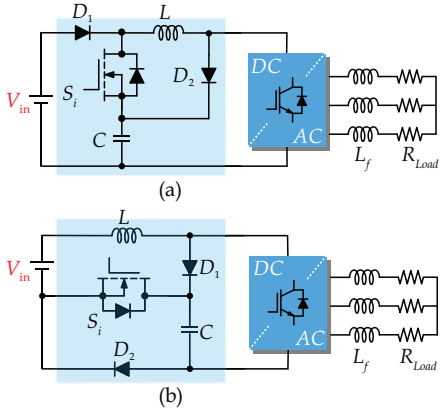

Figure 3. Impedance-source inverter with active power switches: (**a**) switched boost inverter (SBI) [13], and (**b**) embedded-qSBI [14].

Inspired by the above, this paper proposes a modified qZSI with a switched-boost network (S-qZSI), which can achieve continuous input currents and higher boost capability compared with selected switched-boost inverters and modified ZSIs. The rest of this paper is organized as follows. The detailed analysis of the proposed S-qZSI is presented in Section 2. Furthermore, in Section 3, a comprehensive comparison with selected switched-boost ZSIs is carried out and the benchmarking results are provided. The theoretical analysis is verified by simulation and experimental tests in Section 4. Finally, the paper is concluded in Section 5.

2. Operation Principle of the Proposed S-qZSI

The schematic of the proposed S-qZSI is presented in Figure 4. It consists of three capacitors (C_1, C_2, and C_3), three diodes (D_1, D_2, and D_3), two inductors (L_1 and L_2), one power switch (S_1), and a traditional two-level VSI (S_1-S_6). The input voltage is defined as V_{in}. The voltages across the capacitors (C_1, C_2 and C_3) are defined as V_{C_1}, V_{C_2}, and V_{C_3}, and the diode voltages can be expressed as V_{D_1}, V_{D_2}, and V_{D_3}, and the inductor currents are denoted as i_{L_1} and i_{L_2}. Moreover, the load current of phase a is defined as i_a.

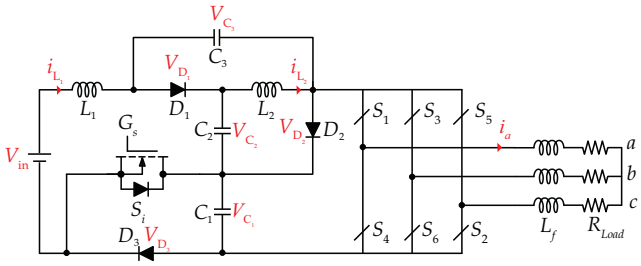

Figure 4. Schematic of the proposed switched-quasi-Z-source inverter.

Similar to the prior-art ZSIs, the boost capability of the proposed S-qZSI can be achieved by utilizing the shoot-through state of the inverter, in which the inverter leg is short-circuited by turning on two switches simultaneously. Therefore, the operation modes of the proposed S-qZSI can be considered as shoot-through mode and non-shoot-through mode, as presented in Figure 5. The corresponding steady-state waveforms are given in Figure 6. In order to simplify the analysis, the capacitors or inductors in the proposed topology are identical.

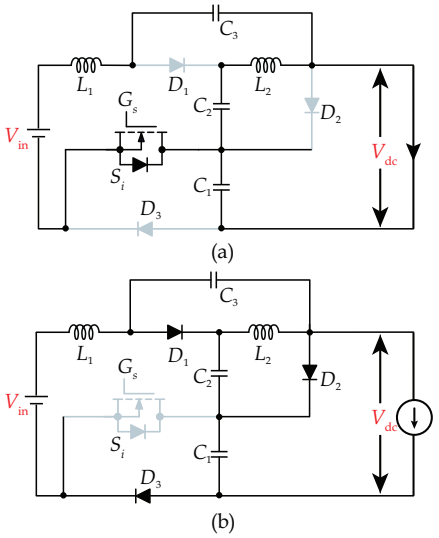

Figure 5. Operation principles of the proposed S-qZSI: (**a**) equivalent circuit during the shoot-through state, and (**b**) equivalent circuit during the non-shoot-through state.

As shown in Figure 5a, if the switches in one of the inverter legs receive the same turn-on signal, the inverter side is short-circuited and the DC-link voltage V_{dc} is zero. The power switch S_1 is in the conduction state due to the turn-on gate signal G_s, as can be seen in Figure 6. Moreover, the diodes D_1, D_2, and D_3 are in OFF-state and the diodes sustain the negative voltage, as presented in Figure 6. Meanwhile, the energy from the input source can be stored in the inductors and the capacitors charge the inductors. Figure 6 shows the inductor currents increase from the minimum to maximum value during the time interval $t_1$to t_2. On the other hand, Figure 5b shows the non-shoot-through mode and the corresponding time interval is t_2 to t_3. In this mode, the operation principle of the inverter is the same as traditional VSI. It can be seen in Figure 6 that the inverter bridge is equivalent to a current source viewed from the DC side [18]. Meanwhile, the switch S_1 is turned OFF and the switch voltage is equal to the voltage of the capacitor C_1. Additionally, all three diodes are ON-state and the voltages of the diodes become zero in Figure 6. Moreover, the inductors can release the stored energy to the load or grid side by controlling the inverter switches. That is, the inductor currents decrease from maximum to minimum value as expected in Figure 6. Accordingly, the voltage and currents across the components can be derived by applying the Kirchhoff's law, as given in Table 1.

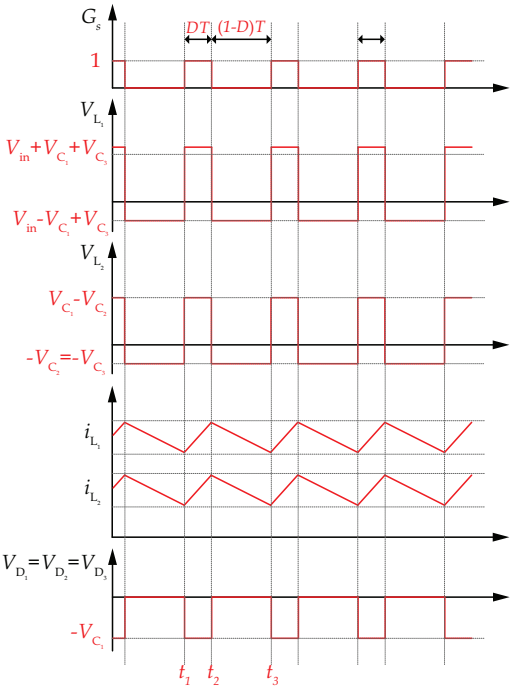

Figure 6. Steady-state waveforms of the proposed S-qZSI.

Table 1. Voltage of the components in shoot-through and non-shoot-through modes.

Components	Voltage	
	Shoot-Through Mode	**Non-Shoot-Through Mode**
Inductor L_1	$V_{C_1}+V_{C_3}+V_{in}$	$V_{in}+V_{C_3}-V_{dc}^{P}$
Inductor L_2	$V_{C_1}-V_{C_2}$	$-V_{C_2}=-V_{C_3}$
Switch S	0	V_{C_1}
Diode D_1	$-V_{C_1}+V_{C_2}-V_{C_3}$	0
Diode D_2	$-V_{C_1}$	0
Diode D_3	$-V_{C_1}$	0
peak DC-link	0	V_{C_1}

The time intervals in the shoot-through mode and non-shoot-through mode can be expressed as DT and $D(1-T)$, where D and T represent the duty cycle and switching period. By applying the volt-second balance principle to the inductors L_1 and L_2, the following can be obtained:

$$D(V_{C_1}+V_{C_3}+V_{in})+(1D)\,(V_{in}+V_{C_3}-V_{dc}^{P})=0 \tag{1}$$

$$D(V_{C_1}-V_{C_2})-(1D)\,V_{C_2}=0 \tag{2}$$

where V_{dc}^{P} is the peak DC-link voltage. Subsequently, the capacitor voltages can be derived as

$$V_{C_1}=\frac{1}{1-3D}V_{in} \tag{3}$$

$$V_{C_2}=V_{C_3}=\frac{D}{1-3D}V_{in} \tag{4}$$

Furthermore, V_{dc}^{p} and boost factor B can be obtained as

$$V_{dc}^{p} = \frac{1}{1-3D} V_{in} = B \cdot V_{in} \tag{5}$$

with

$$B = \frac{1}{1-3D} \tag{6}$$

being the boost factor. Consequently, the voltage gain G in respect to the modulation index M can be expressed as

$$G = MB = \frac{M}{3M-2} \tag{7}$$

3. Comparison with Prior-Art ZSI Topologies

In order to show the performance of the proposed S-qZSI, the component count, boost factor, voltage gain, and component stresses of the proposed S-qZSI and selected topologies are investigated in detail. Firstly, the number of the components in the proposed S-qZSI and selected ZSI topologies is presented in Table 2. According to Table 2, the DA-SBI, CC-qZSI, and the proposed topology all employ two inductors, but the basic SBI and embedded-qSBI only utilize one inductor. Moreover, the quantity of the capacitors in the proposed S-qZSI is higher than the other selected topologies, but it has the same component-count with the DA-ZSI by replacing one diode with a capacitor to construct a quasi-Z-source network.

Furthermore, Table 3 benchmarks the boost factor, voltage gain, and component stresses among the proposed S-qZSI and selected topologies. Figure 7 compares the boost capability of the proposed topology with other selected ZSI/SBIs. In Figure 7a, the comparison between the duty cycle D and the boost factor B for these topologies is presented. It can be seen in Figure 7a that the basic SBI and embedded-qZSI have relatively lower boost capability due to their small component-count. Furthermore, the boost capability of the DA-SBI and CC-qZSI is greatly enhanced by adding more passive components. It is noteworthy that the proposed S-qZSI can achieve a higher boost factor compared with selected topologies in a certain range of shoot-through duty cycles (i.e., 0–0.3), but the component-count of the proposed topology is the same as that of the DA-SBI. Similarly, Figure 7b shows the relationship between the voltage gain and the modulation index. The proposed S-qZSI has the highest voltage gain among the selected topologies if the modulation indexes are identical within the range of 0.68–1. Therefore, the higher modulation index of the proposed S-qZSI results in better power quality for the same voltage output.

In addition to the advantage of the high boost capability, as demonstrated above, the proposed S-qZSI can also achieve lower voltage stresses on the power switches. The detailed voltage stresses expressions for the active switch in the network, inverter bridge switch, the capacitors, and the diodes are presented in Table 3. The voltage stress on the components can be defined as the ratio of voltage across the components to GV_{in}. As shown in Figure 8a, the switch stress of the proposed S-qZSI (see S_i in Figure 6) is lower than that of the SBI and DA-SBI, although the component-count of the proposed S-qZSI and DA-SBI is the same. Moreover, it is noteworthy that the ratio of the CC-qZSI for switch stress is a constant value, which means that the ratio is independent of voltage gain and input voltage. As for the stress comparison of inverter bridge switches (S_1–S_6) as presented in Figure 8b and Table 3, the DA-SBI and CC-qZSI have the same inverter bridge switch stress, and the proposed S-qZSI has the best performance compared with other selected topologies, which allow lower ratings of the switches and reduce the cost to some extent. Moreover, Figure 9a compares the capacitor stress. According to Table 3, two of the capacitors in the proposed S-qZSI have the same voltage stress. Moreover, although the proposed topology utilizes one more capacitor, this additional capacitor has low voltage stress compared with other capacitors based on Table 3. Considering all the topologies in Figure 9a, the CC-qZSI has the lowest capacitor voltage among all the topologies, but the proposed S-qZSI shows

better performance than the SBI, the embedded-qSBI, and the DA-SBI. Finally, the comparison of diode stress is presented in Figure 9b. Similarly, the diode stress of the proposed S-qZSI is much lower than most of the selected topologies, except the embedded-qSBI.

Table 2. Comparison of the number of the components in the proposed Sq-ZSI.

		SBI [13]	Embedded-qSBI [14]	DA-SBI [16]	CC-qZSI [17]	Proposed S-qZSI
Component count	Inductors	1	1	2	2	2
	capacitors	1	1	2	2	3
	switches	1	1	1	1	1
	diodes	2	2	4	2	3

Table 3. Benchmarking of boost factor, voltage gain, and voltage stresses among selected impedance source inverters.

	SBI [13]	Embedded-qSBI [14]	DA-SBI [16]	CC-qZSI [17]	Proposed S-qZSI
Boost factor B	$\frac{1D}{1-2D}$	$\frac{1}{1-2D}$	$\frac{1}{D^2-3D+1}$	$\frac{1}{D^2-3D+1}$	$\frac{1}{1-3D}$
Voltage gain G	$\frac{M^2}{2M-1}$	$\frac{M}{2M-1}$	$\frac{M}{M^2+M-1}$	$\frac{M}{M^2+M-1}$	$\frac{M}{3M-2}$
$\frac{V_{S_1}}{GV_{in}}$	$\frac{1}{G-\sqrt{G^2-G}}+\frac{1}{G}$	$1-\frac{1}{G}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	1	$\frac{3G-1}{2G}$
$\frac{V_{S_2}}{GV_{in}}$	$\frac{1}{G-\sqrt{G^2-G}}$	$2-\frac{1}{G}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	$\frac{3G-1}{2G}$
$\frac{V_{C_1}}{GV_{in}}$	$\frac{1}{G-\sqrt{G^2-G}}$	$2-\frac{1}{G}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}-1$	$\frac{3G-1}{2G}$
$\frac{V_{C_2}}{GV_{in}}$	/	/	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}-1$	1	$\frac{G-1}{2G}$
$\frac{V_{C_3}}{GV_{in}}$	/	/	/	/	$\frac{G-1}{2G}$
$\frac{V_{D_1}}{GV_{in}}$	$\frac{1}{G-\sqrt{G^2-G}}+\frac{1}{G}$	$1-\frac{1}{G}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	$\frac{3G-1}{2G}$
$\frac{V_{D_2}}{GV_{in}}$	$\frac{1}{G-\sqrt{G^2-G}}$	$2-\frac{1}{G}$	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}$	1	$\frac{3G-1}{2G}$
$\frac{V_{D_3}}{GV_{in}}$	/	/	1	/	$\frac{3G-1}{2G}$
$\frac{V_{D_4}}{GV_{in}}$	/	/	$\frac{2G}{1-G+\sqrt{5G^2-2G+1}}-1$	/	/

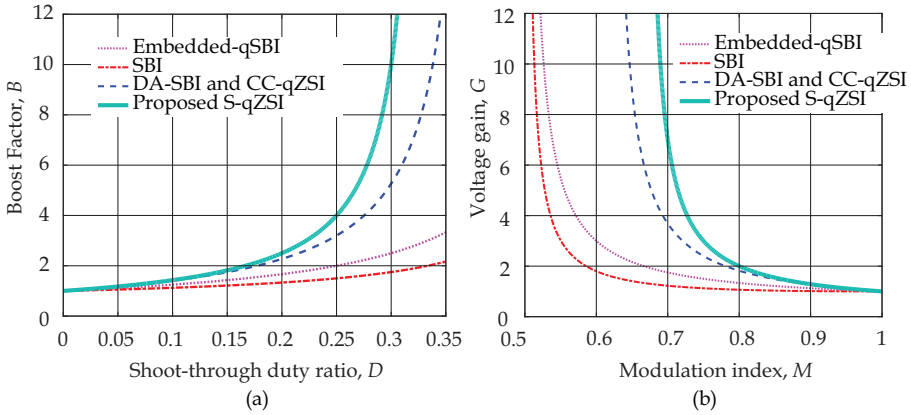

Figure 7. Comparative analysis: (**a**) comparison of the boost factor versus the shoot through duty ratio D among the selected topologies, and (**b**) comparison of the voltage gain versus the modulation index M among the selected topologies.

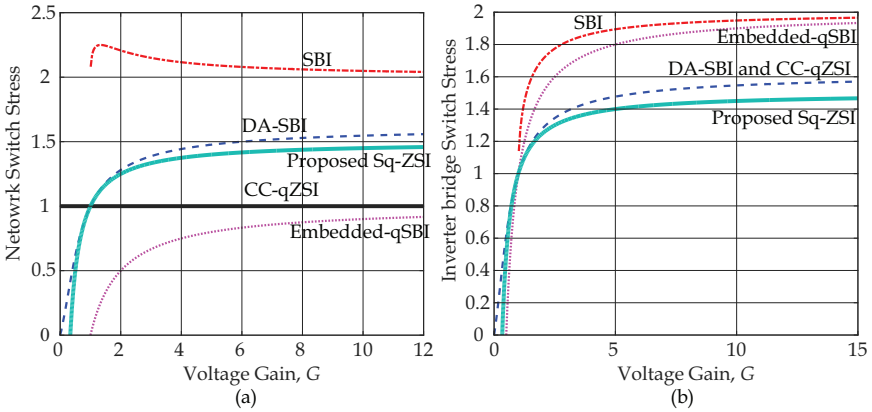

Figure 8. Switch stress comparison among the selected topologies with various voltage gains: (**a**) network switch stress comparison, and (**b**) inverter bridge switch stress comparison.

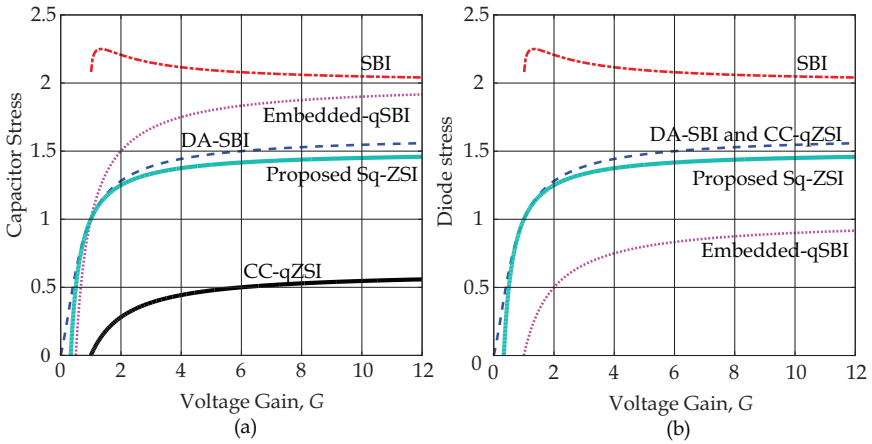

Figure 9. Stress comparison among the selected topologies with various voltage gains: (**a**) capacitor (C_1) stress comparison, and (**b**) diode (D_1) stress comparison.

4. Simulation and Experimental Results

In this section, simulations and experimental tests are provided to verify the performance of the proposed S-qZSI. As shown in Figure 4, the output stage is achieved by a three-phase system for verification. Table 4 presents the system parameters applied in the simulations and experimental prototype.

4.1. Simulation Results

The simulations are executed in the PLECS and Matlab/Simulink platform. The simulation results are given in Figure 10. The output voltage and load current of the whole system are shown in Figure 10a. According to Equation (6), the boost factor B is equal to four when D is 0.25, and thus the DC-link peak voltage can be boosted to 120 V. Figure 10a shows that the DC-link peak voltage is the same as the theoretical value, which equals 120 V. Moreover, the peak load current is about 2 A. Additionally, the DC-link voltage and inductor currents are presented in Figure 10b. It can be seen that the characteristics of the inductor currents match well with the steady-state analysis, where the inductor

currents increase during the shoot-through state and decrease during the non-shoot-through state. It can be observed in Figure 10b that the inductor current i_{L_1} is continuous DC currents. In Figure 10c, the gate signal G_S and diode voltage V_{D_1}, V_{D_2} and V_{D_3} are presented, where the peak diode voltage is the same as the peak DC-link voltage. Figure 10d presents the capacitor voltage of the proposed topology. The voltage of the capacitor C_1 is 120 V, which is equal to the DC-link peak voltage. Moreover, the voltages of the capacitors C_2 and C_3 are only 30 V, which is consistent with the input DC voltage.

Table 4. Parameters of the proposed S-qZSI.

Parameter	Symbol	Value
Modulation index	M	0.83
Duty cycle	D	0.25
DC input voltage	V_{in}	30 V
S-qZSI inductance	L_1, L_2	643 µH
S-qZSI capacitor	C_1, C_2, C_3	100 µF
Load inductance	L_f	3 mH
Load resistance	R_f	40 Ω
Switching frequency	f_s	5 kHz

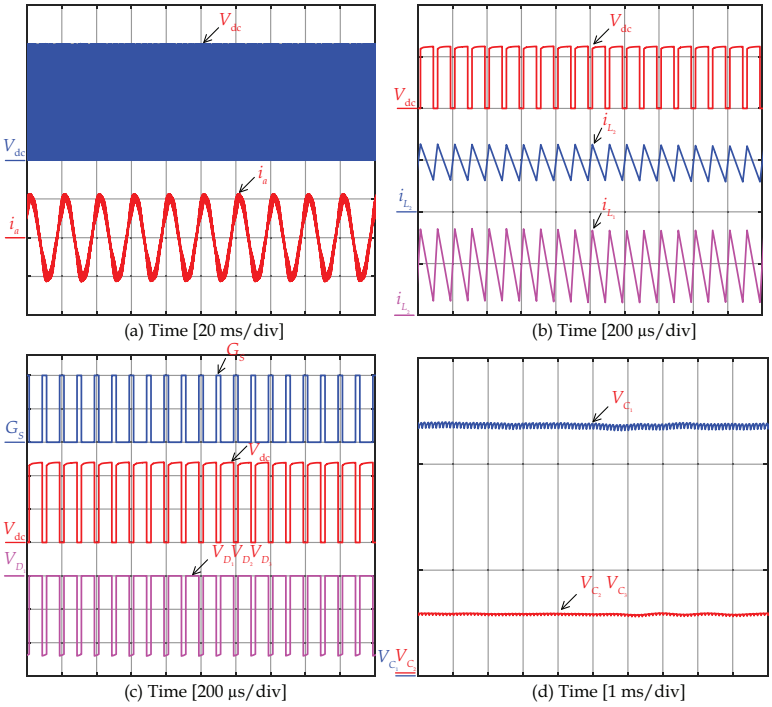

Figure 10. Simulation results of the proposed S-qZSI: (**a**) DC-link voltage V_{dc} [50 V/div] and output phase-a current i_a [2 A/div], (**b**) DC-link voltage V_{dc} [100 V/div] and inductor currents i_{L_1}, i_{L_2} [5 A/div], (**c**) gate signal G_S, DC-link voltage V_{dc} [50 V/div] and diode voltages V_{D_1}, V_{D_2}, V_{D_3} [50 V/div], and **(d)** capacitor voltages V_{C_1}, V_{C_2}, V_{C_3} [50 V/div].

4.2. Experimental Results

The prototype of the proposed S-qZSI is designed based on the previous analysis, as presented in Figure 11. The parameters of the prototype are the same as the parameters applied in the simulations.

The control signals applied in the proposed S-qZSI are generated from a digital signal processor (DSP) TMS320F28335 from Texas Instrument and field-programmable gate array (FPGA) Altera Cyclone 4. The DSP is used to generate the complementary signals and the FPGA board can perform the logical operation based on the output signals from the DSP.

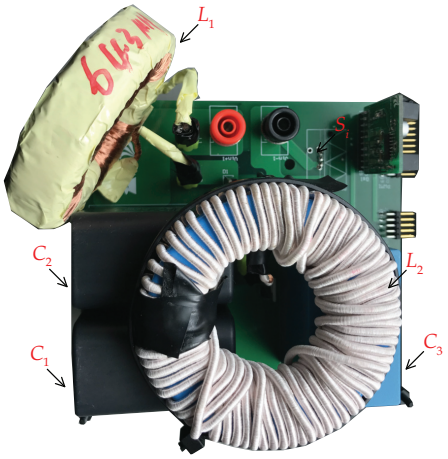

Figure 11. Photograph of the prototype of the proposed S-qZSI.

Figure 12 presents the experimental results of the proposed S-qZSI under the condition that M is 0.83 and D is 0.25. As shown in Figure 12a, the boosted DC-link voltage is approximately 3.88 times as large as the input voltage (30 V) and the load current is about 1.8 A. It can be observed in Figure 12 that the obtained boost factor from the experimental result is slightly lower than the theoretical value due to the parasitic components associated with diodes, switches, capacitors, or inductors applied in the prototype. Moreover, Figure 12b shows the experimental results for the DC-link voltage and inductor currents. It can be observed in Figure 12b that the inductor currents increase linearly in the shoot-through state and decrease linearly in the non-shoot-through state, which is in correspondence with theoretical analysis and simulation results. Meanwhile, the DC-link voltage is zero in the shoot-through state and nonzero in the non-shoot-through state, which matches well with the simulation results. Furthermore, the continuous input current can be ensured in the proposed topology by observing the inductor current i_{L_1}. Additionally, the gate signal G_S and diode voltages are shown in Figure 12c. The peak diode voltage is equal to the peak DC-link voltage. Finally, the capacitor voltages of the proposed topology are shown in Figure 12d. It can be seen that the capacitor voltage V_{C_1} is boosted to 116 V, and it is the same as the DC-link peak voltage. Nevertheless, the capacitor voltages V_{C_2} and V_{C_3} are the same and almost equal to the input voltage (30 V).

In summary, the simulations and experimental results have validated the superior performance of the S-qZSI in terms of high voltage gain, continuous input current, and low voltage stresses on the capacitors.

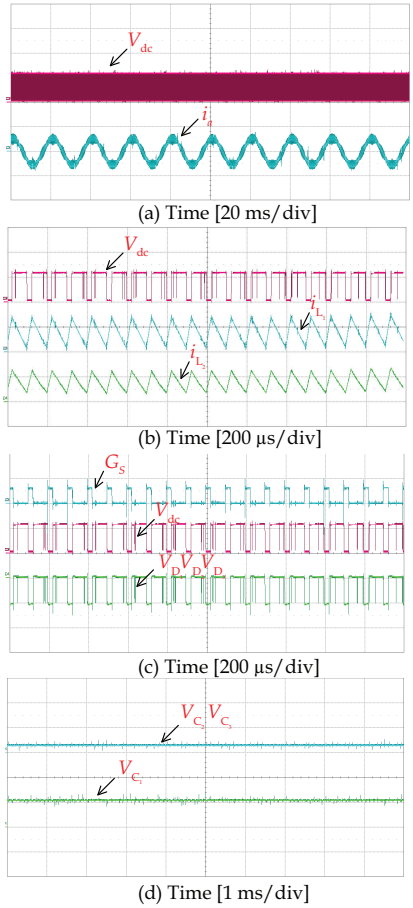

Figure 12. Experimental results of the proposed S-qZSI: (**a**) DC-link voltage V_{dc} [100 V/div] and output phase-a current i_a [2 A/div], (**b**) DC-link voltage V_{dc} [100 V/div] and inductor currents i_{L_1}, i_{L_2} [5 A/div], (**c**) gate signal G_S [20 V/div], DC-link voltage V_{dc} [100 V/div] and diode voltages V_{D_1}, V_{D_2}, V_{D_3} [100 V/div], and **(d)** capacitor voltages V_{C_1}, V_{C_2}, V_{C_3} [100 V/div].

5. Conclusions

This paper has presented a modified switched quasi-Z-source inverter (S-qZSI) based on a switched-impedance network. In the proposed S-qZSI, the boost capability is enhanced by minor modifications compared with other switched-based Z-source networks. Moreover, the proposed S-qZSI features a continuous input current, which makes it suitable for renewable energy applications. In order to show the effectiveness of the proposed S-qZSI, a benchmarking with selected topologies was carried out. The comparison reveals that the voltage stresses of the inverter bridge power switches are lower than the other selected topologies, while the stress of the capacitor remains low. Therefore, the lower rating devices can be utilized to decrease the cost. Finally, the simulation and experimental results shows the superior performance in terms of high boost capability, lower voltage stresses of switches and capacitors, and continuous input currents.

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References

1. Peng, F.Z. Z-source inverter. *IEEE Trans. Ind. Appl.* **2003**, *39*, 504–510. [CrossRef]
2. Yu, Y.; Zhang, Q.; Liang, B.; Liu, X.; Cui, S. Analysis of a single-phase Z-source inverter for battery discharging in vehicle to grid applications. *Energies* **2011**, *4*, 2224–2235. [CrossRef]
3. Anderson, J.; Peng, F.Z. Four quasi-Z-Source inverters. In Proceedings of the 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008; pp. 2743–2749.
4. Yuan, J.; Mostaan, A.; Yang, Y.; Siwakoti, Y.P.; Blaabjerg, F. A Modified Y-Source DC/DC Converter with High Voltage-Gains and Low Switch Stresses. *IEEE Trans. Power Electron.* **2020**. [CrossRef]
5. Mostaan, A.; Yuan, J.; Siwakoti, Y.P.; Esmaeili, S.; Blaabjerg, F. A Trans-Inverse Coupled-Inductor Semi-SEPIC DC/DC Converter With Full Control Range. *IEEE Trans. Power Electron.* **2019**, *34*, 10398–10402. [CrossRef]
6. Serhii, S.; Husev, O.; Vinnikov, D.; Roncero-Clemente, C.; Pimentel, S.; Santasheva, E. Experimental Comparison of Two-Level Full-SiC and Three-Level Si–SiC Quasi-Z-Source Inverters for PV Applications. *Energies* **2019**, *12*, 2509.
7. Honarmand, S.; Rajaei, A.; Shahparasti, M.; Luna, A.; Pouresmaeil, E. A Modified Partial Power structure for Quasi Z-Source Converter to Improve Voltage Gain and Power Rating. *Energies* **2019**, *12*, 2139. [CrossRef]
8. Zhu, M.; Yu, K.; Luo, F.L. Switched Inductor Z-Source Inverter. *IEEE Trans. Power Electron.* **2010**, *25*, 2150–2158.
9. Nguyen, M.; Lim, Y.; Cho, G. Switched-Inductor Quasi-Z-Source Inverter. *IEEE Trans. Power Electron.* **2011**, *26*, 3183–3191. [CrossRef]
10. Li, D.; Loh, P.C.; Zhu, M.; Gao, F.; Blaabjerg, F. Generalized Multicell Switched-Inductor and Switched-Capacitor Z-Source Inverters. *IEEE Trans. Power Electron.* **2013**, *28*, 837–848. [CrossRef]
11. Rostami, S.; Abbasi, V.; Kerekes, T. Switched capacitor based Z-source DC–DC converter. *IET Power Electron.* **2019**, *12*, 3582–3589. [CrossRef]
12. Rostami, S.; Abbasi, V.; Blaabjerg, F. Implementation of a common grounded Z-source DC–DC converter with improved operation factors. *IET Power Electron.* **2019**, *12*, 2245–2255. [CrossRef]
13. Ravindranath, A.; Mishra, S.K.; Joshi, A. Analysis and PWM Control of Switched Boost Inverter. *IEEE Trans. Ind. Electron.* **2013**, *60*, 5593–5602. [CrossRef]
14. Nguyen, M.; Le, T.; Park, S.; Lim, Y. A Class of Quasi-Switched Boost Inverters. *IEEE Trans. Ind. Electron.* **2015**, *62*, 1526–1536. [CrossRef]
15. Ho, A.; Chun, T.; Kim, H. Extended Boost Active-Switched-Capacitor/Switched-Inductor Quasi-Z-Source Inverters. *IEEE Trans. Power Electron.* **2015**, *30*, 5681–5690. [CrossRef]
16. Nozadian, M.H.B.; Babaei, E.; Hosseini, S.H.; Asl, E.S. Steady-State Analysis and Design Considerations of High Voltage Gain Switched Z-Source Inverter With Continuous Input Current. *IEEE Trans. Ind. Electron.* **2017**, *64*, 5342–5350. [CrossRef]
17. Ahmad, A.; Bussa, V.K.; Singh, R.K.; Mahanty, R. Switched-Boost-Modified Z-Source Inverter Topologies With Improved Voltage Gain Capability. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *6*, 2227–2244. [CrossRef]
18. Liu, Y.; Abu-Rub, H.; Ge, B.; Blaabjerg, F.; Ellabban, O.; Loh, P.C. *Impedance Source Power Electronic Converters*; John Wiley & Sons: Hoboken, NJ, USA, 2016.

Journal publication 3

A Modified Y-Source DC/DC Converter with High Voltage-Gains and Low Switch Stresses

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Letters

A Modified Y-Source DC–DC Converter With High Voltage-Gains and Low Switch Stresses

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***Abstract*—This letter proposes a modified Y-source dc–dc converter, which features higher voltage-gains but lower voltage stresses on the components. Moreover, the proposed converter draws a continuous current from the dc input with much control flexibility (i.e., a wide range of adjustable duty cycles). Additionally, the coupled inductors have a low turns ratio, and the core saturation issue is avoided due to the dc-current-blocking capacitor. A detailed analysis of the proposed converter is provided, and the performance is benchmarked with selected coupled-inductors-based converters on various aspects. Experimental tests confirm the theoretical analysis.**

***Index Terms*—DC-DC converter, renewable energy, voltage stress, Y-source converter.**

I. Introduction

DC–DC converters are essential in the grid-integration of PV systems, where a high voltage conversion gain is usually required. Many attempts have thus been made to address the issues associated with conventional high-gain dc–dc converters, e.g., low efficiency for high power applications and high voltage stresses on power devices. On the other hand, extensive topologies for high conversion gains have been introduced in the literature [1]–[3]. Although these converters have high voltage gains, the voltage stress on the power switches is high or equal to the output voltage that can deteriorate the efficiency. Moreover, the adjustable duty cycle range is very limited when requiring a high boost ratio. Finally, the discontinuous current inputs further hinder the applications in the renewable energy applications. Although some modified dc–dc converters have a wide duty cycle and low voltage stresses on the switches, more components are utilized, when compared with conventional topologies [4]–[6].

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Nevertheless, since the introduction of impedance-source converters [7], a vast array of high-gain converters have been developed. It has been proven that the coupled-inductors-based impedance networks can achieve better performances in terms of high voltage-gains and low component-counts [8]–[15]. For instance, the Γ-source impedance networks [8], [9] are typical high-boosting representatives, where coupled-inductors with smaller turns ratios are employed. The Γ-source converter can not only draw a discontinuous current from the dc input but also its adjustable range of duty cycles is limited. Another example among the high voltage-gain impedance-source converters is Y-source-based. The Y-source networks also use lower turns ratio coupled-inductors while offering much flexibility to design the conversion gain [10]–[12]. Unfortunately, similar to the Γ-source networks, the duty cycle for the Y-source networks can only be adjusted in a limited range. Moreover, the switches in these converters are connected to the output voltage side, which leads to high voltage stresses on the switches. In all, either the state-of-the-art solutions are difficult to control (less control flexibility) or there are high stresses on the components.

In light of the above, a modified Y-source-based converter is proposed in this letter. Compared to the prior-art high-gain dc–dc converters, the proposed converter can achieve high voltage-gains with the employment of a low turns-ratio coupled-inductor. More importantly, it can maintain low voltage stresses on the components even for high-voltage applications, and thus contribute to the component selection of smaller power ratings (i.e., lower costs). This distinct feature is achieved by shifting the power device to the input-side with respect to the conventional Y-source converter. The rest of the letter is organized as follows. The operational principles of the proposed dc–dc converter are detailed in Section III, where it is also compared with selected topologies. Experimental tests are performed on a 250-W prototype and the results are provided in Section III, which verifies the theoretical analysis and the superiority of the proposed converter. Finally, concluding remarks are given in Section IV.

II. Proposed Modified Y-Source Converter

A. Operation Principle

The proposed Y-source converter is shown in Fig. 1, which includes an input inductor (L), an active switch (S), two diodes

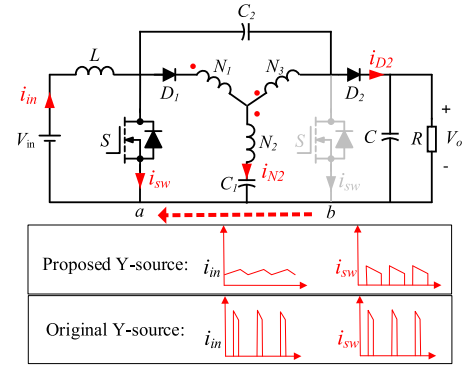

Fig. 1. Schematic of the proposed topology, showing that the power device is moved to the low-voltage side.

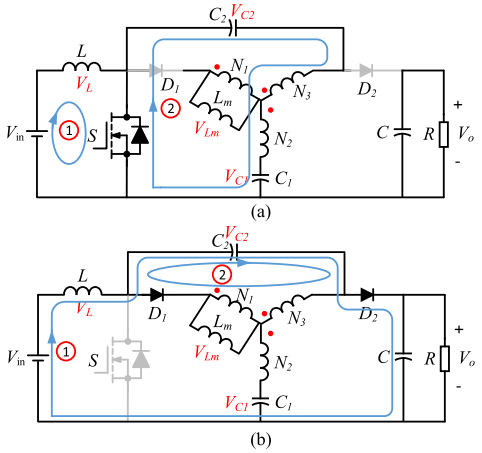

Fig. 2. Equivalent circuits of the proposed topology in: (a) ON-state and (b) OFF-state, where V_x represents the voltage on the component "x" and V_o is the output voltage.

(D_1, D_2), three capacitors (C_1, C_2, C), and a coupled-inductor with three windings (the turns ratios are denoted as N_1, N_2, and N_3). It can be observed in Fig. 1 that the position of the active switch is shifted from the high-voltage side to low-voltage side compared with the conventional Y-source dc–dc converter. In addition, the input current of the proposed converter is continuous and the peak switch current is reduced significantly. It is assumed that the power devices are ideal and the capacitor can maintain the output voltage as a constant. Then, the steady-state conditions of the converter can be analyzed. Clearly, there are two operation states (i.e., S is ON and OFF) in one switching cycle for the proposed converter, as shown in Fig. 2, where the magnetizing inductance is considered. Accordingly, the voltages across the inductor can be obtained as

$$V_{\mathrm{N1}} = V_{\mathrm{Lm}},\quad V_{\mathrm{N2}} = \frac{N_2}{N_1}V_{\mathrm{Lm}},\quad V_{\mathrm{N3}} = \frac{N_3}{N_1}V_{\mathrm{Lm}} \tag{1}$$

where V_{N1}, V_{N2}, V_{N3}, and V_{Lm} are the corresponding voltages on the windings N_1, N_2, N_3, and the magnetizing inductance L_m of the coupled-inductor.

As shown in Fig. 2(a), when S is turned ON, the input inductor L will be charged by the source, and accordingly, the inductor current increases linearly. Moreover, D_1 and D_2 are reverse-biased. Therefore, the capacitor C supplies the load R. According to the Kirchhoff's voltage law (KVL), it can be obtained that

$$V_L - V_{\mathrm{in}} = 0 \tag{2}$$

$$-V_{\mathrm{C2}} - V_{\mathrm{N3}} + V_{\mathrm{N2}} + V_{\mathrm{C1}} = 0 \tag{3}$$

in which V_{in} is the input voltage, V_L is the inductor voltage during the ON-state period, and V_{C1}, V_{C2} represent the capacitor voltage across C_1, C_2, respectively. Substituting (1) into (2) gives the voltage of the magnetizing inductance as

$$V_{\mathrm{Lm}} = \frac{N_1}{N_3 - N_2}\left(V_{\mathrm{C1}} - V_{\mathrm{C2}}\right). \tag{4}$$

When S is turned-OFF, see Fig. 2(b), the energy stored in the inductor L is released to the load through the impedance network. In this case, based on the KVL, the following equations can be obtained as

$$-V_L + V_{\mathrm{in}} + V_{\mathrm{C2}} - V_o = 0 \tag{5}$$

$$-V_{\mathrm{C2}} - V_{\mathrm{N3}} - V_{\mathrm{N1}} = 0. \tag{6}$$

Substituting (1) into (6) leads to the magnetizing voltage as

$$V_{\mathrm{Lm}} = -V_{\mathrm{C2}}\frac{N_1}{N_3 + N_1}. \tag{7}$$

By applying the voltage-second principle to the inductor L and L_m, i.e., (2), (4), (5), and (7), it can be obtained that

$$DV_{\mathrm{in}} + (1-D)\left(V_{\mathrm{in}} + V_{\mathrm{C2}} - V_o\right) = 0 \tag{8}$$

$$D\frac{N_1\left(V_{\mathrm{C1}} - V_{\mathrm{C2}}\right)}{N_3 - N_2} + (1-D)\left(-\frac{N_1}{N_1 + N_3}V_{\mathrm{C2}}\right) = 0 \tag{9}$$

with D being the duty cycle. Finally, the capacitor voltages and the voltage gain G can be expressed as

$$V_{\mathrm{C1}} = V_{\mathrm{in}} + V_{\mathrm{C2}} = \left(1 + \frac{KD}{1-D}\right)V_{\mathrm{in}} \tag{10}$$

$$G = \frac{V_o}{V_{\mathrm{in}}} = \frac{1 + DK}{1 - D} \tag{11}$$

where the winding factor K is expressed as

$$K = \frac{N_3 + N_1}{N_3 - N_2}. \tag{12}$$

To ensure the voltage boosting, it is indicated in (12) that $N_3 > N_2$. The voltage gains for the proposed converter under different turns ratios and various duty cycles are shown in Fig. 3. It can be seen in Fig. 3 that the voltage gain becomes smaller when the turns ratio increases under the same duty cycle. In addition, the range of the duty cycle is much wider than that of the topologies in [8]–[12], as compared in Fig. 4.

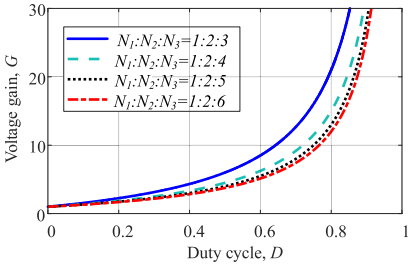

Fig. 3. Voltage gain of the proposed topology for different turns ratio.

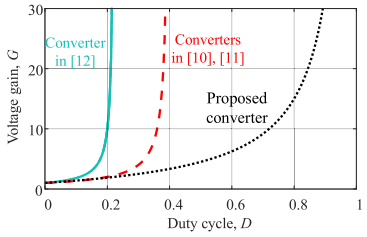

Fig. 4. Voltage gain of the proposed converter and selected converters for the same turns ratio.

B. Design Consideration

As the average capacitor current and the average magnetic inductor voltage are zero in one switching cycle. The average currents i_{N_1}, i_{N_2}, and i_{N_3} through winding the three windings are

$$i_{N_1} = \frac{N_3}{N_1} i_o, \quad i_{N_2} = 0, \quad i_{N_3} = i_o \tag{13}$$

where i_o is the output current. Based on the Kirchhoff's current law (KCL), it can be obtained that

$$i_{Lm} = i_{N_1} + i_{N_3} = \left(1 + \frac{N_3}{N_1}\right) i_o \tag{14}$$

with i_{Lm} being the magnetizing current. During the ON-state the magnetizing current flows to the winding N_1, and therefore, i_{N_2} and i_{N_3} are equal with together

$$i_{N_2(ON)} = i_{N_3(ON)}. \tag{15}$$

By using the ampere turn balance in the windings, we have

$$N_1 i_{N_1} + N_2 i_{N_2} = N_3 i_{N_3}. \tag{16}$$

Then, it can be obtained that

$$i_{N_2(ON)} = i_{N_3(ON)} = \frac{N_1}{N_3 - N_2} i_{N_1(ON)}. \tag{17}$$

In addition, i_{N_2} flows through C_1 and i_{N_3} flows through C_2, and thus the capacitors voltage ripples can be obtained as

$$\Delta v_{C_1} = \frac{N_1 i_{Lm}}{N_3 - N_2} \cdot \frac{D}{C_1 f}, \ \Delta v_{C_2} = \frac{N_1 i_{Lm}}{N_3 - N_2} \cdot \frac{D}{C_2 f} \tag{18}$$

in which f is the switching frequency. Therefore, the capacitor values can be calculated according to (18). Moreover, the output capacitor can be obtained as

$$C = \frac{i_o D}{\Delta v_C f} \tag{19}$$

where Δv_C is the voltage ripple of the output capacitor. The design of the coupled inductor is similar to the original Y-Source network [10], so the minimum value of the magnetizing inductance can be derived as

$$L_m = \frac{N_1 \left(V_{C2} - V_{C1}\right) D}{2 i_o \left(1 + \frac{N_3}{N_1}\right) \left(N_3 - N_2\right) f}. \tag{20}$$

C. Voltage Stress Analysis

To further assist the component selection, the voltage stresses over the active switch, diodes, and capacitors are analyzed. Notably, the voltage stress is defined as the ratio of the voltage across the corresponding component to the input voltage.

When S is OFF, the voltage $V_{\rm sw}$ across the switch can be obtained as

$$V_{\rm sw} = V_o - V_{\rm C2}. \tag{21}$$

By substituting (10) and (11) into (13), the voltage stress can be derived as

$$\frac{V_{\rm sw}}{V_{\rm in}} = \frac{G + K}{1 + K} = \frac{1}{1 - D}. \tag{22}$$

It is clear that the voltage stress of the switch is only determined by the duty cycle. When S is ON, the voltage stresses of the diodes can be obtained as

$$\frac{V_{d_1}}{V_o} = \frac{K^2 + KG + 2\,K}{1 + KD}, \ \frac{V_{\rm d_2}}{V_{\rm in}} = \frac{G + K}{1 + K}. \tag{23}$$

Based on the above, the suitable semiconductors can be chosen according to K and the required output voltage. Moreover, the capacitor stresses can be derived according to (10)

$$\frac{V_{\rm C1}}{V_{\rm in}} = \frac{KG + 1}{K + 1}, \ \frac{V_{\rm C2}}{V_{\rm in}} = \frac{KG - K}{K + 1}. \tag{24}$$

D. Comparison With Selected Topologies

A comprehensive comparison between the proposed converter and selected topologies is summarized in Table I, where n is the turns ratio. It can be observed in Table I that the Γ-source converter has the lowest component-count among the benchmarked. However, the discontinuous input current is its main drawback. Although the modified Γ-source converter in [9] can draw a continuous input current, the duty cycle control range is narrow, as aforementioned. Compared to the Γ-source networks, the Y-source networks have a three-winding structure. The Y-source converter in [12] uses many components to achieve a higher voltage gain, which leads to an increased cost. Furthermore, although the converters in [10]–[12] have a better boost capability, the duty cycle is limited in a narrow range, which is also indicated in Fig. 4. This means that the control is very sensitive to the duty cycle, when a high voltage-gain is required. Although the converters in [4]–[6] have a wide duty cycle range, they have more components than the proposed converter. In addition, the input current ripple in [4] and [6] is high, which

TABLE I
BENCHMARKING OF SELECTED TOPOLOGIES BASED ON COUPLED INDUCTORS

Converters in	[4]	[5]	[6]	[8]	[9]	[10]	[11]	[12]	Proposed
Counts of inductors + coupled inductors	0+2	1+2	4+0	0+2	1+2	0+3	1+3	2+3	1+3
Counts of capacitors	4	5	1	2	3	2	3	5	3
Counts of switches	1	1	2	1	1	1	1	1	1
Counts of diodes	4	4	7	2	2	2	2	3	2
Input current ripple	high	low	high	high	low	high	low	low	low
Duty-cycle control range	$0<D<1$	$0<D<1$	$0<D<1$	$0<D<\frac{1}{1+\frac{1}{n-1}}$	$0<D<\frac{1}{2+\frac{1}{n-1}}$	$0<D<\frac{1}{K}$	$0<D<\frac{1}{K}$	$0<D<\frac{1}{K+2}$	$0<D<1$

n is the turns-ratio and K is coefficient defined in (12).

TABLE II
COMPARISON OF VOLTAGE STRESSES OVER THE COMPONENTS AMONG SELECTED Y-SOURCE CONVERTERS

Voltage stress	Y-source [10]	quasi-Y-source [11]	Proposed Y-source
C_1	$\frac{4G+1}{5}$	$\frac{4G+1}{5}$	$\frac{5G+1}{6}$
C_2	/	$\frac{4G-4}{5}$	$\frac{5G-5}{6}$
D_1	$4G$	$4G$	$\frac{4G+25}{6}$
D_2	G	G	$\frac{G+5}{6}$
S	G	G	$\frac{G+5}{6}$

makes them inappropriate in renewable energy systems. In all, among the benchmarked topologies, the proposed converter can achieve superior performances (i.e., continuous input current, high voltage-gain, and wide duty-cycle control range).

Furthermore, the voltage stress across the capacitors, diodes, and switches among Y-source, quasi-Y-source and the proposed converter is compared by setting the winding factor to five, which is summarized in Table II. According to Table II, the voltage stresses of the capacitors among the proposed topology, Y-source and quasi-Y-source converter are very close, which means that the capacitor voltage stress is not affected by changing the position of the active switch. In addition, the voltage stresses over the diodes and switch in the proposed topology are significantly reduced. That is when a large voltage gain is needed, the proposed modified Y-source converter. This is beneficial to the device selection for high dc output voltages, thus, minimizing the cost.

III. EXPERIMENTAL VERIFICATION

A 250-W experimental prototype is built to verify the theoretical analysis.

The parameters of the prototype are listed in Table III. For the coupled-inductor, the windings are designed with 20, 12, and 20 turns in an interleaved structure to minimize the leakage inductance. The winding factor K is 5 and duty cycle is chosen as 0.6 to achieve a voltage gain of 10 for the proposed converter. A commercial dc source (ITECH IT6522 C DC Power Supply) was used in the experiments, and the converter supplied a passive load. Experimental results are shown in Fig. 5. The control and modulation were implemented in a digital signal processor (TMS320F28335).

As it is shown in Fig. 5(a), the output voltage V_o under the open-loop control is about 390 V, which matches the expected

TABLE III
DESIGN PARAMETERS OF THE PROPOSED CONVERTER

Parameter/Description	Value/Part Number
Rated Power	250 W
Input/Output Voltage	40/400 V
Capacitor/Input Inductor	100 μF/640 μH
Turns-Ratio	20:12:20
Core	B66397G0000X197
Switching Frequency	100 kHz
Duty Cycle	0.60
Switch S	IPP60R099C6XKSA1
Diode D_1&D_2	IDP30E65D2XKSA1

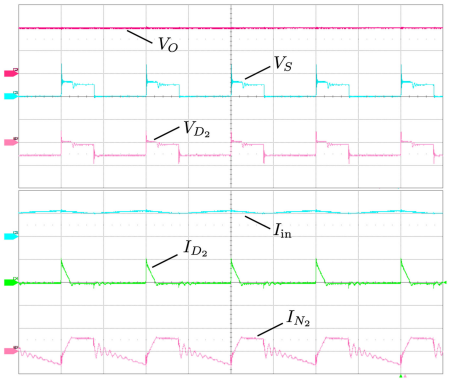

Fig. 5. Experimental results of the proposed converter operating at 200 W (output voltage V_o [200 V/div], switch voltage V_S [200 V/div], voltage of D_2 V_{D_2} [200 V/div], input current I_{in} [5 A/div], current of D_2 I_{D_2} [10 A/div], secondary current I_{N_2} [10 A/div], time [5 μs/div]).

theoretical value–400 V. Moreover, observations in Fig. 5(a) indicate that the input current I_{in} is continuous with low ripples and the mean value is about 5.4 A, meaning that the proposed converter draws a continuous current from the dc input. Therefore, the continuous input current and high voltage gain make the proposed Y-source converter more suitable for renewable energy applications, where a large conversion ratio is required. Moreover, it can be seen in Fig. 5(a) that the current flowing in the secondary winding of the coupled-inductor is a periodic signal without dc currents. This is because the capacitor C_1 in series with the coupled-inductor winding can prevent the magnetic core saturation.

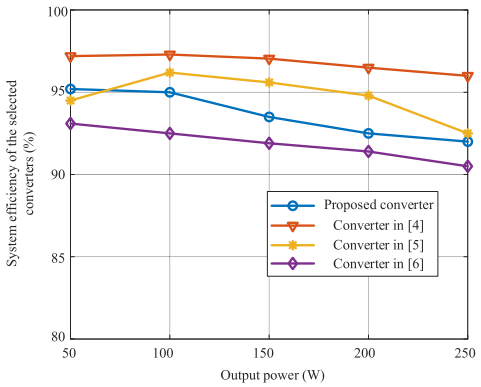

Fig. 6. Efficiency comparison of the selected dc–dc converters.

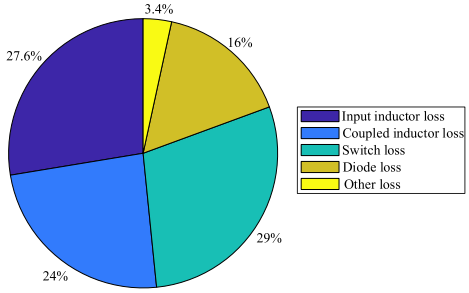

Fig. 7. Power loss distribution of the modified Y-source dc–dc converter.

More importantly, the voltage stress V_S over the active switch S is 110 V, which is much lower than the output voltage. Especially, the voltage spike shown in Fig. 5(b) is lower than the output voltage. This is in agreement with the previous analysis that the voltage stress of the active switch is significantly reduced compared with other Y-source converters. Similarly, the voltage V_{D_2} across the diode D_2 is about 110 V. As for the diode current I_{D_2}, it decreases from its maximum to zero during the turn-OFF state. Therefore, D_2 is working under the zero current switching (ZCS), which is beneficial to the converter efficiency.

Additionally, the efficiency of the proposed topology is measured with a high precision power analyzer (PPA5530). The efficiency of the converter under various loading conditions is shown in Fig. 6. The output power varies from 50 to 250 W for a constant input voltage (i.e., 40 V). It can be observed in Fig. 6 that the overall efficiency of the converter is above 92% at the rated power of 250 W and the peak efficiency is 95.2%. Notably, as compared in Fig. 6 the dc–dc converters in [4], [5] have a better efficiency, but both utilize more components than the proposed converter, leading to an increased cost. Moreover, it should be pointed out that the converter in [4] requires an LC filter in its input to limit the high frequency current ripples. Although more components are used in [6], its efficiency is lower than the proposed converter when the voltage gain is 10.

In addition, as shown in Fig. 7, the coupled-inductor and the input inductor account for a large proportion of the total losses of the proposed converter. Thus, the optimization of the proposed converter and the application of efficient power devices (e.g., gallium nitride devices) as the main active switch may also contribute to the efficiency improvement, which will be future work.

IV. Conclusion

In this letter, a modified Y-source dc–dc converter with a high voltage-gain has been proposed. The high voltage-gain can be flexibly achieved by setting the proper turns ratio of the coupled-inductor. Moreover, the proposed converter has a wide adjustable range of the duty cycle and it can draw a continuous current from the input source. One key feature of the proposed converter is that the voltage stress on the active switch is much lower compared with its counterparts. This allows the adoption of low power rating devices (e.g., gallium nitride devices) for high-voltage inverter applications, while maintaining low costs. Experimental tests have validated the effectiveness of the proposed dc–dc converter.

References

[1] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-source networks for electric power conversion part I: A topological review," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 699–716, Feb. 2015.

[2] M. H. B. Nozadian, E. Babaei, S. H. Hosseini, and E. Shokati Asl, "Switched Z-source networks: A review," *IET Power Electron.*, vol. 12, no. 7, pp. 1616–1633, Jul. 2019.

[3] F. M. Shahir, E. Babaei, and M. Farsadi, "Extended topology for a boost DC-DC converter," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2375–2384, Mar. 2019.

[4] L. Schmitz, R. F. Coelho, and D. C. Martins, "High step-up high efficiency DC-DC converter for module-integrated photovoltaic applications," in *Proc. 13th Brazilian Power Electron. Conf. 1st Southern Power Electron. Conf.*, Nov. 2015.

[5] R. Moradpour, H. Ardi, and A. Tavakoli, "Design and implementation of a new SEPIC-based high step-up DC/DC converter for renewable energy applications," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1290–1297, Feb. 2018.

[6] Y. Tang, D. Fu, T. Wang, and Z. Xu, "Hybrid switched-inductor converters for high step-up conversion," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1480–1490, Mar. 2015.

[7] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar. 2003.

[8] P. C. Loh, D. Li, and F. Blaabjerg, "Γ-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4880–4884, Nov. 2013.

[9] W. Mo, P. C. Loh, and F. Blaabjerg, "Asymmetrical Γ-source inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 637–647, Feb. 2014.

[10] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, and G. E. Town, "Y-source impedance network," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3250–3254, Jul. 2014.

[11] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "Quasi-Y-source boost DC-DC converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6514–6519, Dec. 2015.

[12] Y. Wang *et al.*, "A family of Y-source DC/DC converter based on switched inductor," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1587–1597, Mar. 2019.

[13] M. Nguyen, Y. Lim, J. Choi, and Y. Choi, "Trans-switched boost inverters," *IET Power Electron.*, vol. 9, no. 5, pp. 1065–1073, 2016.

[14] S. S. Nag and S. Mishra, "A coupled inductor based high boost inverter with sub-unity turns-ratio range," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7534–7543, Nov. 2016.

[15] A. R. Majarshin and E. Babaei, "High step-up DC-DC converter with reduced voltage and current stress of elements," *IET Power Electron.* vol. 12, no. 11, pp. 2884–2894, Sep. 2019.

Journal publication 4

A Trans-Inverse Coupled-Inductor Semi-SEPIC DC/DC Converter with Full Control Range

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Letters

A Trans-Inverse Coupled-Inductor Semi-SEPIC DC/DC Converter With Full Control Range

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***Abstract*—This letter proposes a single switch magnetically coupled dc–dc converter with a high voltage gain. The unique features of the converter are summarized as follows: 1) voltage gain of the converters is raised by lowering its magnetic turn ratio; 2) wide control range ($0 < D < 1$); 3) continuous current from the source that makes it a suitable candidate for renewable energy applications; and 4) there is no dc current saturation in the core due to the presence of capacitor in the primary winding of the inductor. The feasibility of the proposed converter is studied in details supported by circuit analysis and simulation results. Furthermore, the proposed converter is analyzed and compared with other converters with similar features. Finally the superior performance of the circuit is validated experimentally.**

***Index Terms*—Coupled inductor, dc–dc converter, regenerative snubber, renewable energy, SEPIC, voltage stress.**

I. Introduction

RENEWABLE energy resources such as photovoltaic (PV), wind, and fuel cell are being widely employed in recent years to decrease the negative side effects of conventional energy resources. However, the renewable energy resources usually cannot be directly connected to the grid because of their intermittent nature. As an example, the low and variable dc-input voltage (20–45 V) generated from the PV modules should be boosted enough to high voltage (e.g., 200–400 V), in order to generate ac utility voltage using dc–ac converter. Similarly, in hybrid electric vehicle (HEV) and other electric traction systems, a voltage of 14 or 42 V from batteries, fuel cells, and/or super capacitors needs to be raised to 200 or 500 V during various modes of operation [1]. The requirement for dc voltage boosting is even more prominent lately with the emergence of the 400 V microgrids powered by multiple energy sources, and the introduction of facility-level 400 V dc distribution for data and telecommunication centers. Therefore, high step-up dc–dc converters play a vital role in renewable energy systems [1], [2]. Conventional boost converters have very simple structures, where its theoretical voltage gain reaches infinitely when the duty cycle is near to unity. Meanwhile, due to higher losses at elevated duty cycle, the practical voltage gain cannot exceed 4–5 even with a well-designed layout [3]. To overcome this issue of limited voltage gain in the conventional boost converter, different solutions have been presented in the literature [4]–[15]. Switch inductor, switch capacitor; multicell and cascaded configurations [4]–[6] are well investigated to achieve a higher voltage gain. However, to achieve a high voltage gain, several switched inductor/capacitor cells are typically required, resulting in higher cost, size, and complexity [7]. Coupled inductor technique is an interesting method to achieve high voltage gain using less number of components [8], [9]. Usually in most converters with this technique, the voltage gain can be increased by increasing the coupled inductor turn ratio, which may lead to a higher cost and size [10]. Moreover, usually an additional snubber circuit is required to dissipate the leakage energy of the coupled inductors, which creates the voltage spike across the switch. This leads to a more complex circuit with lower overall efficiency [7]. Recently, coupled inductor converters in a series based on impedance-source networks have been introduced such as Γ-source [11], Y-source [12], and improved Γ-source [13]. In these converters, the voltage gain is increased by lowering the coupled inductor turn ratio, which provides a great advantage in reducing the overall size of the converter for a higher voltage gain. However, these converter demands higher voltage rated switch with higher $R_{\mathrm{DS(ON)}}$ (equal or higher than the output voltage) resulting in a higher power loss. In addition, by lowering the coupled inductor turn ratio, the useful range of the duty cycle to achieve practical voltage gain is narrowed down. This results in a very steep voltage gain, which complicates the converter control because of greater sensitivity of the output voltage to the duty cycle [10]. Two trans-inverse converters were presented in [10] and [14] with a high voltage gain and much lower voltage stress on the switch, however similar to converters in [11]–[13] the duty cycle operates in a narrow range. A new trans-inverse converter is proposed in [15] where the duty cycle can vary between 0 and 1 without a very steep voltage gain curve, however,

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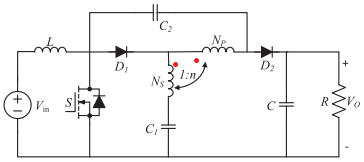


Fig. 1. Schematic of the proposed converter.

its input current has a high ripple that makes it inappropriate for PV application, where low input current ripple is preferred. To mitigate the aforementioned problems, a novel trans-inverse converter is presented in this letter with continuous input current with very low ripple magnitude. Its duty cycle variation range is between 0 and 1 without very high steep gain curve. In addition, the voltage stress on the switch is much lower than the output voltage. Furthermore, it does not require any external snubber circuit, where the leakage energy is recycled by a built-in regenerative snubber circuit and finally the dc-current saturation of the core is prevented because of the presence of the dc current blocking capacitor in series with one of the transformer windings. This letter is organized as follows: in Section II, the converter is analyzed in details in a continuous conduction mode (CCM). The performance of the converter is verified using simulation and experimental results in Section III and the findings drawn are finally concluded in Section IV.

II. Proposed Trans-Inverse Converter

A. Description of the Converter in CCM

The schematic of the proposed converter is shown in Fig. 1. Similar to the conventional single-ended primary-inductor converter (SEPIC), it consists of an input inductor (L), one common ground switch (S), an intermediate capacitor (C_2), output diode (D_2), and output capacitor (C). With some modifications, the intermediate inductor in the SEPIC converter is replaced with an impedance network, which consists of one diode (D_1), one capacitor (C_1), and coupled inductors, where $n = N_P/N_s$ indicates their turn ratio. To simplify the analysis, the following assumptions are made: 1) All components are ideal that means all equivalent series resistance in inductors and capacitors are neglected. In addition, the forward voltage drop of the diodes, drain-source on resistance $R_{DS(ON)}$, and parasitic capacitances of the switch (S) are negligible. 2) All capacitors are large enough where the voltage across them is constant in one switching cycle. 3) The coefficient of the transformer coupling is one, which means the leakage inductances are zero. However, the leakage inductances effect on the voltage spike across the power switch will be considered in the next section. With above assumptions, there are two stages in one switching cycle as shown in Fig. 2. When the power switch turns ON as shown in Fig. 2(a), both diodes become reverse bias and turned OFF. The input inductor charges through the input source and the output load is isolated from the source and is powered by the output capacitor. As it can be seen from Fig. 2(a), we can write

$$V_{\mathrm{LM}} = \frac{V_{C1} - V_{C2}}{n-1}. \tag{1}$$

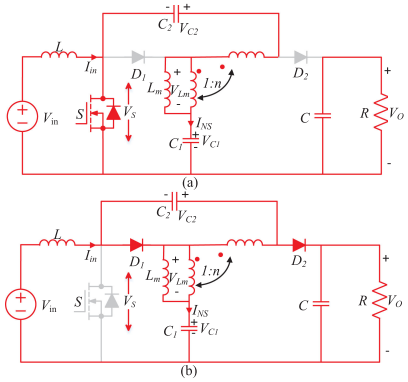


Fig. 2. Equivalent circuits of the proposed converter when the switch turns (a) ON and (b) OFF.

Both diodes are forward biased when the switch is turned OFF as shown in Fig. 2(b). The input inductor releases its energy to the load, where its current decreases and the output capacitor is charged from the input source. In this stage, the circuit expressions are given as follows:

$$V_{\mathrm{LM}} = \frac{V_{C1} - V_O}{n-1}. \tag{2}$$

Applying volt-second balance principle to input inductor and magnetizing inductor, they can be obtained as

$$DV_{\mathrm{in}} + (1-D)(V_{\mathrm{in}} - V_{C2} - V_O) = 0 \tag{3}$$

$$D\left(\frac{V_{C2} - V_{C1}}{n-1}\right) + (1-D)\left(\frac{V_{C1} - V_O}{n-1}\right) = 0. \tag{4}$$

By some derivations, the voltage gain across C_1, C_2, and output voltage are obtained as

$$V_{C1} = \left(1 + \frac{nD/(n-1)}{1-D}\right) V_{\mathrm{in}}\ V_{C2} = \left(\frac{nD/(n-1)}{1-D}\right) V_{\mathrm{in}}$$
$$V_O = G \cdot V_{\mathrm{in}} = \left(\frac{1 + nD/(n-1)}{1-D}\right) V_{\mathrm{in}} \tag{5}$$

where G is the voltage gain of the proposed converter. Refer to (5) and Fig. 3, it is clear that the converter gain increases when the turns ratio decreases. However, the duty cycle range can vary in a wide range ($0 < D < 1$), unlike converters presented in [10]–[13] where the range of duty cycle is narrow.

B. Inbuilt Voltage Clamp Circuit

In practice, the leakage inductance is nonzero and may cause large voltage spikes on the power switch due to resonance with the switch parasitic capacitor. However, in the proposed converter when the power switch is turned OFF, both diodes are turned ON. Refer to Fig. 2(b); the switch voltage is clamped to difference of output voltage and capacitor voltage V_{C2}. Therefore, using capacitors C_1, C_2, and diode D_1 and D_2, we make an

TABLE I
COMPARISON WITH STATE-OF-THE-ART TOPOLOGIES

Converter	[10]	[11]	[12]	[13]	[14]	[15]	Proposed
Num. of inductors+ couple inductors	1+2	0+2	0+3	1+2	1+2	0+2	1+2
Num. of capacitors	5	2	2	3	5	3	3
Num. of switches	1	1	1	1	1	1	1
Num. of diodes	4	2	2	2	4	3	2
Input current ripple	low	high	high	low	low	high	low
DC current block capacitor	yes	yes	yes	yes	no	no	yes
Switch voltage stress($\frac{v_s}{v_o}$)	$\frac{n-1}{2(n-1)+D}$	1	1	1	$\frac{n-1}{2n-1}$	$\frac{n-1}{2n-1}$	$\frac{n-1}{2n-1}$
Duty cycle variation range	$0<D<\frac{n-1}{n}$	$0<D<\frac{1}{1+\frac{1}{n-1}}$	$0<D<\frac{1}{K}$	$0<D<\frac{1}{2+\frac{1}{n-1}}$	$0<D<\frac{n-1}{2n-1}$	$0<D<1$	$0<D<1$

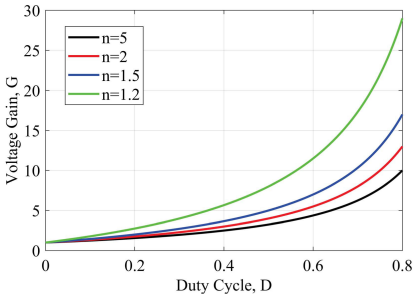


Fig. 3. Voltage gain of the proposed converter in Fig. 1.

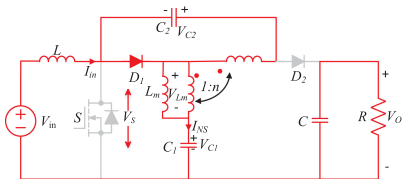


Fig. 4. Equivalent circuits of the proposed converter when the diode D_2 is turned OFF in stage 2.

inbuilt regenerative snubber circuit that helps to redirect the leakage energy safely to the power capacitors. With this arrangement, the requirement of additional lossy snubber circuit is eliminated.

C. Effect of the Leakage Inductance on the Converter Performance

The coupled inductor was considered as an ideal to perform the steady-state analysis; however, when the effect of the leakage inductance is considered in analysis, the diode D_2 turned OFF before the end of the switching cycle. However, when its effects are considered, diode D_2 is turned OFF before the end of the stage 2. Therefore, in addition to Fig. 2(b), there is another equivalent circuit in stage 2, which diode D_2 is turned OFF as shown in Fig. 4.

With high coupling coefficient in the coupled inductor design ($K \approx 1$), the leakage inductance value is small in comparison with the magnetizing inductance. With this assumption and using voltage-second principle law on input inductor and magnetizing inductance in Figs. 2 and 4, the voltage across C_1, C_2, and output voltage is the same as (5). Therefore, the reverse bias of the diode D_2 in stage 2 does not have considerable effect on the converter performance and its voltage gain. This is verified later in the experimental results section.

D. Comparison With Similar Topologies

Table I presents a comparison of the proposed converter with several trans-inverse type converter. Γ-source [11] and Y-source [12] have the lowest number of components; however, their input current is discontinuous with high ripple magnitude that makes them inappropriate in renewable energy systems. Converters in [10] and [13] have continuous input current with low ripple, but the duty cycle variation range is narrow particularly when n tends to unity, which complicates the controller design because of higher sensitivity of the output voltage to duty ratio. In addition, the voltage stress on the switch is high and equal to output voltage in the presented converters in [11]–[13].

The duty cycle can vary in a wide range as presented in [15]; however, the input current ripple in this converter is high, therefore, an input filter is mandatory in renewable energy systems that makes its structure more complicated. Compared with [15], the input current ripple in the proposed converter is low and also one diode is saved in the proposed converter compared with [15]. Moreover one dc current block capacitor in series with one coupled inductor can prevent from core saturation in the proposed converter. Compared to converters in [10]–[13], it has a wide range of duty cycle variations for any coupled inductor turn ratio and therefore lower sensitivity to D. In addition, it benefits from low voltage stress on switch in comparison with [11]–[13]. Fig. 5 shows the static voltage gain of the proposed converter and presented converters in [10] and [14] for n = 1.5. Converters in [10], [11], and [14] have a high voltage gain. However, the duty cycle cannot exceed than 1/3 in [10] and [11] and 1/4 in [14].

Therefore, the duty cycle variation range is narrow and voltage gain varies steeply that makes their control more complicated. In addition, some diodes in [10] and [14] conduct in only a small portion of the switching cycle, which results in a reverse recovery problem. In contrast, the voltage gain variation in the proposed converter is smooth that simplifies its control. From the number of components viewpoint, refer to Table I, the converters in [10] and [14] have more number of components compared to the proposed converter.

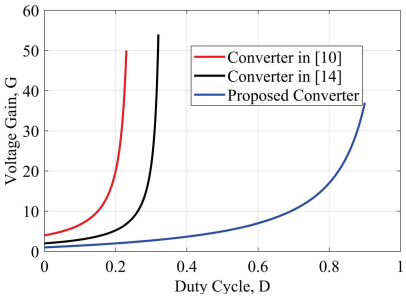


Fig. 5. Voltage gain comparison of the proposed converter and converters in [10] and [14] for n = 1.5.

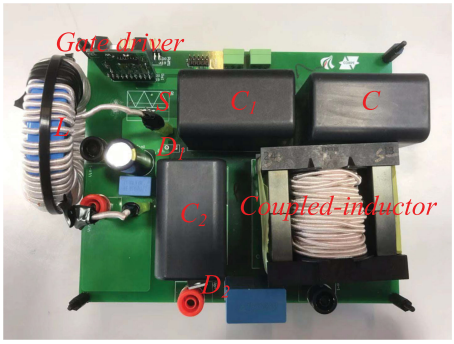


Fig. 6. Picture of the hardware prototype.

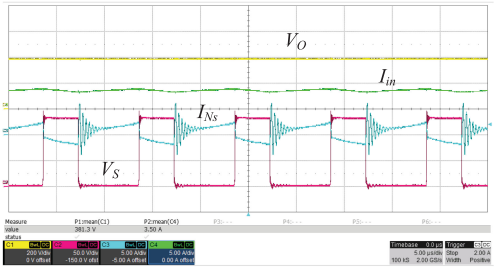
TABLE II
DESIGN PARAMETERS OF THE PROPOSED CONVERTER

Parameter/Decription	Value/Part Number
Power rating	150-400 W
Input/Output voltage	48/400 V
Capacitor/input inductance	100 μF/640 μH
Turn ratio	28:20 Core:B66397G0000X197
Leakage/magnetizing inductance	1.27/220 μH
Switching frequency	100 kHz
Duty Cycle	0.62
Switch S	IPP60R099C6XKSA1
Diode D1&D2	IDP30E65D2XKSA1

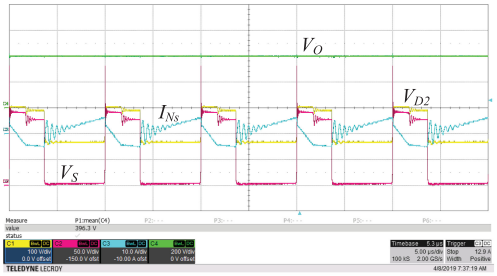
III. EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, a prototype is built as shown in Fig. 6. The circuit parameters of the proposed converter are listed in Table II. Fig. 7(a) shows the experimental results under 168 W output power. The output voltage is about 400 V under open-loop control. It is clear that the proposed converter is able to boost the 48 V input voltage to higher voltage with an acceptable ripple. The input current mean value is 3.5 A. It is obvious that the input current is continuous with a low ripple.

The voltage stress on the power switch is about 130 V, which is much lower than the output voltage. It is clear that there is no



(a)



(b)

Fig. 7. Experimental results obtained at (a) Po: 168 W. (b) Po: 325 W. Output voltage (200 V/div), input current (5 A/div), and switch voltage (50 V/div) and coupled inductor secondary current (5 A/div) and diode D_2 voltage (100 V/div).

voltage spike across the power switch that confirms the theoretical analysis. Finally, that figure shows the current that flowing in the transformer secondary winding, it has a periodic signal with no dc current because the capacitor C_1 in series with transformer winding can prevent from core saturation. Experimental results under output power 325 W are shown in Fig. 7(b). Under open-loop control, the output voltage is about 396.3 V, which is much closer to its theoretical value. This confirms that the effect of leakage inductance on the converter performance and its voltage gain is small. The voltage stress on diode D_2 is about 130 V [Ch2 of Fig. 7(b)], which is much lower than the output voltage. In addition, this diode is turned OFF before the end of second stage because of the leakage inductance effect as seen in the theoretical analysis in Section II-C. In this case, the voltage stress on the switch is lower than the output voltage. The efficiency of the proposed converter is measured at different output power levels from 50 to 400 W as shown in Fig. 8. The converter efficiency at all output power level is above 92% and its maximum value is 94% at full load (400 W), which confirms that high efficiency can be achieved using the proposed converter.

The loss distribution of the proposed converter at Po = 325 W is shown in Fig. 9. The major loss is related to magnetic elements (input inductor and coupled inductors). The second power loss comes from the power switch that consists of the switching loss and conduction loss. The power loss on diodes is about 12% of the power loss. Other loss is 7% that mainly consists of the capacitor loss.

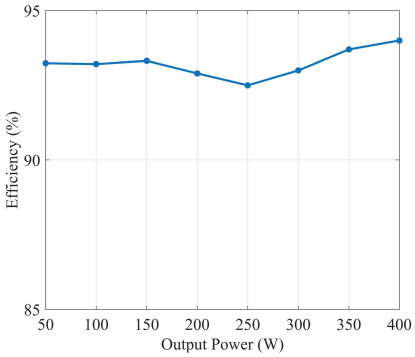


Fig. 8. System efficiency at varying load (Vin = 48 V, D = 0.62, fs = 100 kHz).

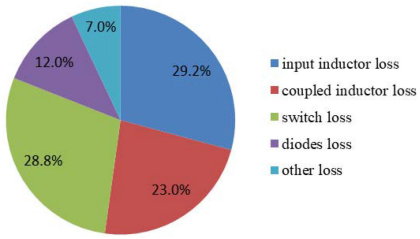


Fig. 9. Power loss distribution.

IV. Conclusion

A new coupled inductor-based semi-SEPIC converter is introduced in this letter. The voltage gain of the converter increases by lowering the coupled inductors turn ratio, which may lead to a lower size and cost. Unlike most trans-inverse type converters, the duty cycle in the proposed converter can vary in wide range, which simplifies the controller design. In addition, the converter draws a continuous current from the source with low ripple magnitude that makes it suitable for renewable energy applications. In addition, a dc blocking capacitor in series with coupled inductor can prevent from core saturation. These demonstrated performances clearly stands out the proposed topology as a competitive alternative for a practical application where a high voltage gain is demanded, such as for fuel cells and PVs.

References

[1] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[2] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans Power Electron*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[3] A. Mostaan, A. Abdelhakim, M. Soltani, and F. Blaabjerg, "A switched-boost DC/DC converter with high voltage gain and continuous input current," in *Proc. Annu. Appl. Power Electron. Conf. Expo.*, Mar. 2018, pp. 1540–1545.

[4] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC-DC PWM converters," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 2, pp. 687–696, Mar. 2008.

[5] Y. Tang, D. Fu, T. Wang, and Z. Xu, "Hybrid switched-inductor converters for high step-up conversion," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1480–1490, Mar. 2015.

[6] F. L. Tofoli, D. de Souza Oliveira, R. P. Torrico-Bascop, and Y. J. A. Alcazar, "Novel nonisolated high-voltage gain DC-DC converters based on 3SSC and VMC," *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 3897–3907, Sep. 2012.

[7] Y. P. Siwakoti *et al.*, "High voltage gain quasi-SEPIC DC-DC converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1243–1257, Jun. 2019.

[8] J. Yao, A. Abramovitz, and K. M. Smedley, "Analysis and design of charge pump-assisted high step-up tapped inductor SEPIC converter with an inductorless regenerative snubber," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5565–5580, Oct. 2015.

[9] K. Tseng, J. Lin, and C. Huang, "High step-up converter with three-winding coupled inductor for fuel cell energy source applications," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 574–581, Feb. 2015.

[10] Y. P. Siwakoti, F. Blaabjerg, and P. Chiang Loh, "High step-up trans-inverse (Tx^{-1}) DC-DC converter for the distributed generation system," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4278–4291, Jul. 2016.

[11] P. C. Loh, D. Li, and F. Blaabjerg, "Γ-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4880–4884, Nov. 2013.

[12] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, S. J. Andreasen, and G. E. Town, "Y-source boost DC/DC converter for distributed generation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 1059–1069, Feb. 2015.

[13] W. Mo, P. C. Loh, and F. Blaabjerg, "Asymmetrical Γ-source inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 637–647, Feb. 2014.

[14] H. Liu, J. Wang, and Y. Ji, "A novel high step-up coupled-inductor DC-DC converter with reduced power device voltage stress," *IEEE J. Emerg. Sel. Topics Power Electron.*, p. 1, 2018, doi: 10.1109/JESTPE.2018.2868769.

[15] H. Liu, F. Li, and P. Wheeler, "A family of DC-DC converters deduced from impedance source DC-DC converters for high step-up conversion," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6856–6866, Nov. 2016.

Journal publication 5

Analysis and Design of a High Voltage Gain Quasi-Z-Source DC-DC Converter

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Abstract: In this study, a modified DC–DC converter is proposed, which can achieve a high voltage-gain exploiting both quasi-Z-source and switched-capacitor networks. In addition to the high voltage-gain, the proposed converter has low voltage stresses on its elements. The steady-state analysis in both continuous and discontinuous conduction modes is given in this study. Moreover, the design of the passive elements, the calculation of the non-ideal voltage gain, and the power loss analysis are done. Then, an extended topology of the proposed converter is presented, which further enhances the voltage gain, while maintaining the voltage stresses of the components. A comprehensive comparison with the prior-art converters is performed to accentuate the advantages of the proposed converter. Finally, simulations and experimental tests are provided to substantiate the theoretical analysis.

1 Introduction

High voltage-gain DC–DC converters have a wide range of applications, e.g. in fuel cells, wind and photovoltaic systems [1], and electric drives [2]. High gain DC–DC converters can be categorised into two major categories: isolated and non-isolated. Isolated converters employ transformers to achieve the high voltage-gain and the galvanic isolation between the input and the output. In this kind of converters, the voltage gain can be enhanced readily by increasing the turns ratio of the transformers. However, a high number of components, high power losses, and the transformer saturation possibility may degrade the performance of the converters [3]. Conventional non-isolated converters have lower voltage gains, simpler circuits, and higher efficiency compared to the isolated ones [4]. To compensate for the low voltage-gain of non-isolated DC–DC converters, many techniques and structures have been introduced in the literature. Certain commonly-used techniques to increase the voltage gain of converters are cascaded topologies [5], voltage-lift (VL) cells [6], switched-capacitors (SC) [7], switched-inductors (SL) [8], multiplier cells [9], Z-source (ZS) networks [10], quasi-ZS (qZS) networks [11], switched-boost (SB) networks [12], quasi-SB (qSB) networks [13], and coupled inductors [14–16]. Although the combination of these techniques can further multiply the voltage gain, it will inevitably increase the complexity and the cost of the converter. For instance, in [14–16], high voltage-gain and efficiency can be obtained by regulating the turns ratio of the coupled inductors. However, in some cases, using coupled inductors lead to high input current ripples and delayed diode reverse recovery time.

Furthermore, a qZS DC–DC converter has employed a VL cell in [17], which leads to a high boosting capability of up to five in low duty cycles. Nonetheless, high voltage stresses on semiconductors and more inductors in the converter are the main drawbacks. The converter in [18] can achieve a high voltage-gain with a high number of elements, simultaneously, utilising the combination of the qZS network and the cascading technique. Likewise, in [19], a high voltage-gain converter has been introduced, which employs a qZS network and a voltage multiplier cell. However, it shows the same disadvantage of the cascading technique, i.e. a high number of components. The qZS DC–DC converters in [20, 21] employ the SL and SC networks in the conversion, respectively, to enhance the voltage gain. However, the voltage gain improvement is not remarkable in these converters. Furthermore, the converter in [22] employs two SC networks and one energy storage cell to enhance the voltage gain. Nonetheless, this combination increases the complexity of the converter and the number of its elements. Moreover, a modified ZS converter is introduced in [23], which shows a higher voltage gain compared to the conventional ZS converter. However, the voltage gain improvement is not significant, and it shows high voltage stress on its elements. In [24], although the combination of a qZS network and quadratic boost converter is used to modify the voltage gain, its voltage gain is the same as the conventional ZS converter. Similarly, a combination of an SC network and regenerative boost configuration is represented in [25] to achieve high boosting capabilities. This converter achieves high voltage gains with a high duty cycle close to one. Both SC-SB and SCSL-SB converters have been presented in [26] with low voltage stress on capacitors. However, many inductors and diodes are required for these topologies. The modified qZS DC–DC converter in [27] presents a higher voltage gain compared to the conventional qZS DC–DC converter. On the contrary, it requires a high number of capacitors and diodes in its topology. Although the presented qZS converter in [28] can achieve high voltage gains, its circuit demands a high number of passive elements. In [29], two high-gain DC–DC converters are presented using two and three qZS networks. However, these converters have the same drawback of the presented converter in [28]. The converters in [26–29] use a high number of elements and some of them have limited boosting capability.

In this paper, a modified SC-qZS DC–DC converter with a high boosting capability, the low voltage stress on its elements and continuous input current is proposed. The primitive version of this converter with limited analysis was presented in [30]. The calculation of the non-ideal voltage gain, power loss analysis, steady-state analysis in the discontinuous conduction mode (DCM), an extended topology and experimental results are further discussed in this paper. More specifically, in Section 2, the operation principle and the component design are presented, which is followed by the non-ideal voltage gain and the power loss analysis. The steady-state analysis in the DCM is given in Section 3. The proposed converter is compared with the prior-art solutions in Section 4. Simulations and experimental tests have been presented in Section 5, and the results validate the effectiveness of the proposed converter. Finally, concluding remarks are provided in Section 6.

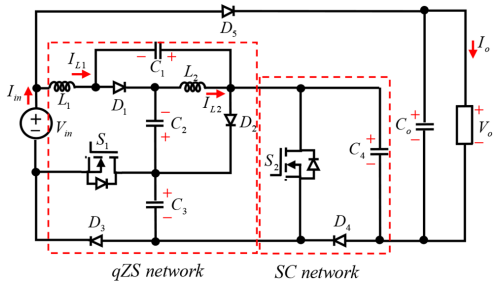

Fig. 1 *Proposed high step-up DC–DC converter*

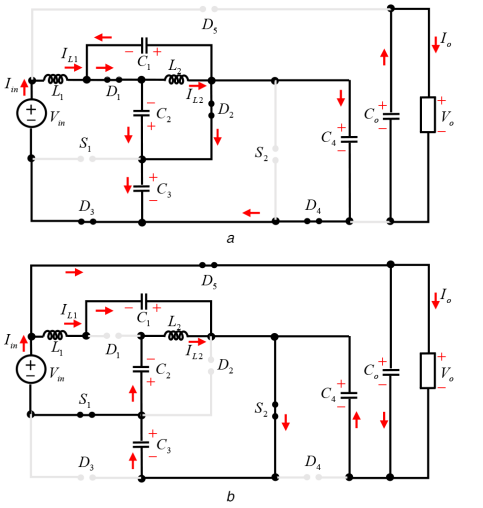

Fig. 2 *Equivalent circuits of the proposed converter in the CCM*
(a) Mode 1, ***(b)*** Mode 2

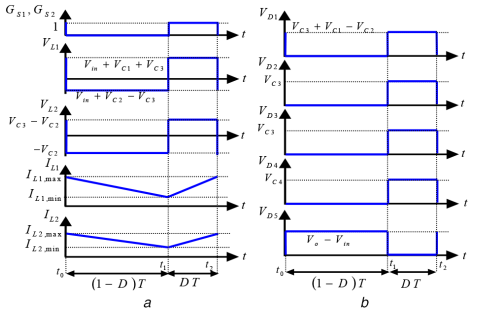

Fig. 3 *Steady-state waveforms of the proposed converter in the CCM*
(a) Gating pulses of the switches, voltages across and currents flowing through the inductors, ***(b)*** Voltages across the diodes

2 Proposed converter and its CCM operation

In Fig. 1, the proposed converter is demonstrated, which is obtained using the modified qZS network (inductors L_1 and L_2, capacitors C_1, C_2 and C_3, diodes D_1, D_2 and D_3, and switch S_1) and the SC network (switch S_2, diode D_4, and capacitor C_4). In addition to these networks, the diode D_5 and the capacitor C_o are other elements of the proposed DC–DC converter. When operating in the continuous conduction mode (CCM), the proposed converter has two modes as shown in Fig. 2. In the following, the operation modes, the component design (inductors and capacitors), the non-ideal gain and the power losses are discussed for the converter in the CCM.

2.1 Operation modes

Mode 1 in the CCM $[t_0 \le t < t_1]$: In the first operating mode, the switches S_1, S_2 and the diode D_5 are off, while the diodes D_1, D_2, D_3 and D_4 are conducting. As a consequence, C_1, C_3 and C_4 are charging, where L_1, L_2 and C_2 are discharging. Therefore, the following equations are valid:

$$V_{L1} = V_{\text{in}} + V_{C2} - V_{C3}, V_{L2} = -V_{C2}, V_{C1} = V_{C2}, V_{C3} = V_{C4} \quad (1)$$

$$I_{\text{in}} = I_{L1}, i_{C1} + i_{C2} = I_{L2} - I_{L1}, i_{C3} + i_{C4} = I_{L1} \quad (2)$$

$$V_{S1} = -V_{C3}, V_{S2} = -V_{C4}, V_{D5} = V_{\text{in}} - V_{\text{o}} \quad (3)$$

in which, V_{C1}, V_{C2}, V_{C3} and V_{C4} are voltages of C_1, C_2, C_3 and C_4, respectively, and V_{in} and V_{o} indicate the input and output voltages, respectively. Furthermore, V_{L1} and V_{L2} are voltages of L_1 and L_2, respectively. I_{L1} and I_{L2} indicate currents of L_1 and L_2, respectively, i_{C1}, i_{C2}, i_{C3} and i_{C4} represent currents of C_1, C_2, C_3 and C_4, respectively, and I_{in} presents the input current. V_{S1} and V_{S2} are voltages of S_1 and S_2, respectively. Moreover, the voltage of D_5 is denoted as V_{D5}.

Mode 2 in the CCM $[t_1 \le t < t_2]$: In this mode, all the components have a reverse condition compared to the first mode. For example, S_1, S_2 and D_5 are on, where D_1, D_2, D_3 and D_4 are off. As a result, although L_1, L_2 and C_2 are charging, C_1, C_3 and C_4 are in the discharging mode. The following equations can then be obtained:

$$\begin{cases} V_{L1} = V_{\text{in}} + V_{C3} + V_{C1}, V_{L2} = V_{C3} - V_{C2}, \\ V_{\text{o}} = V_{\text{in}} + V_{C3} + V_{C4} \end{cases} \quad (4)$$

$$\begin{cases} i_{C1} = -I_{L1}, i_{C2} = I_{L2}, i_{C3} = -I_{\text{in}} - I_{L2}, \\ i_{C4} = I_{L1} - I_{\text{in}}, I_{L1} = I_{\text{in}} - I_{\text{o}} \end{cases} \quad (5)$$

$$V_{D1} = V_{C2} - V_{C1} - V_{C3}, V_{D2} = V_{D3} = -V_{C3}, V_{D4} = -V_{C4} \quad (6)$$

where V_{D1}, V_{D2}, V_{D3} and V_{D4} indicate the voltages of D_1, D_2, D_3 and D_4, respectively. At the end of the second mode in the CCM, the switching period ends. Fig. 3 demonstrates the steady-state waveforms of the proposed DC–DC converter in the CCM. The pulse width modulation (PWM) is used to control gating signals of switches. As can be observed from Fig. 3, the gating pulses of S_1 and S_2 are the same. The voltages of capacitors and the voltage gain equation in the CCM can be extracted considering the volt-second balance law of the inductor and Fig. 3 as:

$$\begin{cases} V_{C1} = V_{C2} = \dfrac{DV_{\text{in}}}{(1-3D)}, V_{C3} = V_{C4} = \dfrac{V_{\text{in}}}{(1-3D)} \\ G_{\text{CCM}} = \dfrac{V_{\text{o}}}{V_{\text{in}}} = \dfrac{3(1-D)}{(1-3D)} \end{cases} \quad (7)$$

with D being the duty cycle and G_{CCM} indicating the voltage gain of the proposed converter operating in the CCM. Based on (7), the proposed converter achieves high voltage gains in low duty cycles while also maintaining low voltage stress on capacitors. Fig. 4 shows the extended type of the proposed converter. One capacitor and one diode are applied in the extended topology, which increases the voltage gain of the converter without increasing the voltage stress on capacitors and switches. The operation of the extended topology is similar to the main proposed topology in Fig. 1. The extended converter has two operating modes. In the first mode, S_1, S_2 and D_6 are conducting and other diodes are

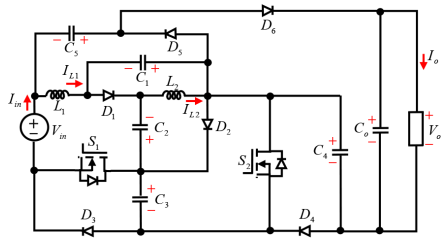

Fig. 4 *Extended high gain converter based on the proposed converter*

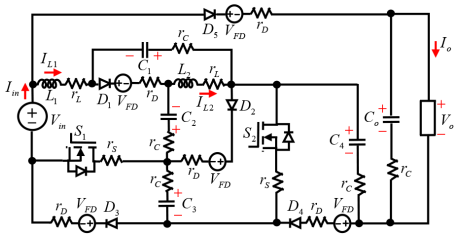

Fig. 5 *Schematic diagram of the proposed converter with parasitic elements*

reversed biased. In the second mode, D_1, D_2, D_3, D_4 and D_5 are conducting, while S_1, S_2 and D_6 are off. The equations and mathematical calculations to obtain the voltage gain and voltages across capacitors in the extended topology are the same as the proposed converter in Fig. 1. Thus, only the derived results have been provided in this section as follows to avoid repetition. That can be expressed as follows:

$$\begin{cases} V_{C1,\text{extended}} = V_{C2,\text{extended}} = \dfrac{\text{DV}_{\text{in}}}{1-3D} \\ V_{C3,\text{extended}} = V_{C4,\text{extended}} = \dfrac{V_{\text{in}}}{1-3D} \\ V_{C5,\text{extended}} = \dfrac{3\text{DV}_{\text{in}}}{1-3D}, G_{\text{extended}} = \dfrac{V_{\text{o}}}{V_{\text{in}}} = \dfrac{3}{1-3D} \end{cases} \tag{8}$$

where the subscript 'extended' indicates the variables in the extended topology.

2.2 Passive components design

To design the inductor, the current ripple of the inductor is required. Considering (1), (7) and $V_L = L\text{d}i/\text{d}t$, the current ripple is expressed as

$$\Delta I_{L1} = \frac{2D(1-D)V_{\text{in}}}{L_1 f_s (1-3D)} \tag{9}$$

where f_s indicates the switching frequency. The current ripple of L_2 can be derived in a similar way as

$$\Delta I_{L2} = \frac{D(1-D)V_{\text{in}}}{L_2 f_s (1-3D)} \tag{10}$$

Additionally, the average value of the inductor current is also required. This average value for the inductor current will be obtained by applying the Kirchhoff's Current Law in Fig. 1 and considering (7), which is

$$I_{L1,\text{ave}} = I_{\text{in}} - I_{\text{o}} = \frac{G^2 V_{\text{in}}}{R} - \frac{\text{GV}_{\text{in}}}{R} = \frac{6(1-D)}{R(1-3D)^2} V_{\text{in}} \tag{11}$$

$$I_{L2,\text{ave}} = I_{L1,\text{ave}} \tag{12}$$

in which G is the voltage gain and R is the load resistance. Thus, the inductors can be designed by substituting (9)–(12) in the inductor current ripple factor as

$$L_1 = 2L_2 = \frac{RD(1-3D)}{3x_{L1}\%f_S} \tag{13}$$

with $x_L\% = \Delta I_L / I_{L,\text{ave}}$. Similarly, the capacitor voltage ripple can be derived by substituting (5), (11) and (12) in $I_C = C\text{d}V_C/\text{d}t$, which gives

$$\begin{cases} \Delta V_{C1} = \Delta V_{C2} = \dfrac{3D(1-D)\left(3D^2-4D+3\right)V_{\text{in}}}{C_{1\text{or}2} f_s R(1-3D)^2} \\ \Delta V_{C3} = \dfrac{3D(1-D)\left(3D^2-7D+6\right)V_{\text{in}}}{C_3 f_s R(1-3D)^2} \\ \Delta V_{C4} = \dfrac{3D^2(1-D)V_{\text{in}}}{C_4 f_s R(1-3D)} \end{cases} \tag{14}$$

where ΔV_{C1}, ΔV_{C2}, ΔV_{C3} and ΔV_{C4} are voltage ripples of capacitors. Thus, the capacitors can be obtained by substituting (7) and (14) in the voltage ripple factor as

$$\begin{cases} C_{1,2} = \dfrac{3(1-D)\left(3D^2-4D+3\right)}{x_{C1,2}\%f_s R(1-3D)} \\ C_3 = \dfrac{3D(1-D)\left(3D^2-7D+6\right)}{x_{C3}\%f_s R(1-3D)} \\ C_4 = \dfrac{3D^2(1-D)}{x_{C4}\%f_s R} \end{cases} \tag{15}$$

with x_{C1}, x_{C2}, x_{C3} and x_{C4} being the ripple factor of capacitors C_1, C_2, C_3 and C_4 and $x_C\% = \Delta V_C / V_C$.

2.3 Non-ideal voltage gain analysis

The ideal voltage gain of the proposed converter in the CCM is obtained in (7) by neglecting the effect of the parasitic elements. In this section, the real voltage gain of the proposed converter is obtained considering the parasitic elements. To achieve the real voltage-gain in the CCM, Fig. 5 is used. To simplify the analysis, the inductor internal resistance is considered identical. The same assumption is done for switches, diodes and capacitors. In the time interval of $(1–D)T$, the non-ideal voltages of the proposed converter can be expressed as

$$\begin{cases} v_{L1} = V_{\text{in}} - r_L I_{L1} - V_{FD} - \dfrac{r_D I_{L1}}{1-D} + V_{C2} - \left(\dfrac{r_C I_{L1} D}{(1-D)}\right) \\ -V_{C3} - r_C(I_{\text{in}} - I_{\text{o}}/1-D) - r_D I_{\text{in}} - V_{FD} \\ v_{L2} = -V_{FD} - V_{C2} + \left(\dfrac{D(r_C I_{L1} - r_D I_{\text{in}})}{1-D}\right) \\ V_{C1} = V_{C2} + \left(\left(\dfrac{Dr_D I_{\text{in}} - r_D I_{L1} - 2r_C I_{L1} D}{1-D}\right)\right) \\ V_{C4} = V_{C3} + r_C I_{\text{in}} + \left(\dfrac{(Dr_D I_{\text{in}} - I_{\text{o}}(r_C + r_D + 1))}{1-D}\right) \end{cases} \tag{16}$$

Likewise, in the time interval of DT, the voltages can be obtained that

$$\begin{cases} v_{L1} = V_{\text{in}} - r_L I_{L1} + V_{C1} - r_C I_{L1} + V_{C3} + (r_S + r_C)\left(I_{\text{in}} - \left(\dfrac{I_{L1}}{D}\right)\right) \\ v_{L2} = -r_L I_{L2} + V_{C3} - V_{C2} - r_C I_{L2} + (r_S + r_C)\left(I_{\text{in}} - \left(\dfrac{I_{L1}}{D}\right)\right) \\ V_o = V_{\text{in}} + V_{C3} + V_{C4} - V_{FD} - r_D(I_{\text{in}} - I_{L1}) - \left(\dfrac{r_S I_{L1}}{D}\right) \\ + r_C\left(I_{\text{in}} + 2I_{L1} - \left(\dfrac{2I_{L1}}{D}\right)\right) \end{cases} \tag{17}$$

in which r_L and r_C are the internal resistance of the inductor and the capacitor, respectively, r_S is the internal resistance of the switch and r_D is the internal resistance of the diode. In addition, V_{FD} indicates the voltage drop of the diode. Using (16), (17) and the volt-second balance law, the real voltage gain of the proposed converter is then be obtained as (see (18)) . The comparison between the ideal and real voltage gains of the proposed converter is demonstrated in Fig. 6.

2.4 power loss analysis

In this section, the power loss analysis of the proposed converter in the CCM is presented. The conduction loss of components, P_{Cond}, can be obtained as

$$P_{\text{Cond}} = \left(\frac{1}{T}\right)\int_0^T (V_F I + rI^2)\mathrm{d}t \tag{19}$$

where T is the switching period, V_F is the voltage drop of the element, r is the internal resistance of the element and I is the current flowing through the component. Therefore, substituting the steady-state equations obtained in previous sections into (19) leads to the total conduction losses of components as

$$\begin{cases} P_{\text{Cond, switches}} = \left(\dfrac{r_S G^2 V_{\text{in}}^2}{R^2}\right)\left[\dfrac{[G(1-D)-1]^2 + G^2 D^2}{D}\right] \\ P_{\text{Cond, diodes}} = \dfrac{r_D G^2 V_{\text{in}}^2}{R^2}\left[\dfrac{G^2(2D^2 - 2D + 2) - 2G + 2 + D - D^2}{1-D}\right] \\ +\left(\dfrac{V_{\text{FD}} G(2G + D)V_{\text{in}}}{R}\right) \\ P_{\text{Cond, capacitors}} = \dfrac{r_C G^2 V_{\text{in}}^2}{R^2}\left[\dfrac{1 + (1-D)^2 + 2D(G-1)^2}{1-D} + \right. \\ \left. \dfrac{(2D-1)^2(G-1)^2}{D} + \dfrac{[1 - G(1-D)]^2}{D(1-D)}\right] \\ P_{\text{Cond, inductors}} = \dfrac{2r_L G^2 (G-1)^2 V_{\text{in}}^2}{R^2} \end{cases} \tag{20}$$

where $P_{\text{Cond,switches}}$, $P_{\text{Cond,diodes}}$, $P_{\text{Cond,capacitors}}$ and $P_{\text{Cond,inductors}}$ are the total conduction losses of switches, diodes, capacitors and inductors, respectively. The switching loss of the semiconductors, P_{SW}, is obtained as

$$P_{\text{SW}} = V_S I_S (t_r + t_f) f_S \tag{21}$$

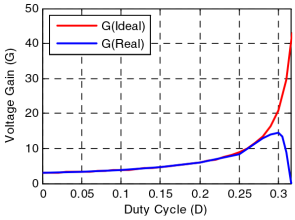

Fig. 6 *Comparison of the ideal and real voltage gains of the converter*

in which V_S and I_S are the drain-source voltage and current, respectively, and t_r and t_f are the rise and fall time of switches. Consequently, considering (21) and the steady-state equations in the CCM, the total switching losses of semiconductors can be calculated as

$$P_{\text{SW, switches}} = \frac{G(G-1)V_{\text{in}}^2(t_{rs} + t_{fs})f_S}{6RD(1-3D)} \tag{22}$$

$$P_{\text{SW, diodes}} = \frac{2G(G+1-D)V_{\text{in}}^2(t_{rd} + t_{fd})f_S}{6R(1-D)(1-3D)} \tag{23}$$

Summing the conduction loss and the switching loss results in the total power loss as:

$$\begin{aligned} P_{\text{Loss, total}} = {} & P_{\text{Cond, switches}} + P_{\text{Cond, diodes}} + P_{\text{Cond, capacitors}} \\ & + P_{\text{Cond, inductors}} + P_{\text{SW, switches}} + P_{\text{SW, diodes}} \end{aligned} \tag{24}$$

Thus, the efficiency is given as

$$\eta = \frac{(P_{\text{in}} - P_{\text{total loss}}) \times 100}{P_{\text{in}}} \tag{25}$$

with η indicating the efficiency, P_{in} being the input power and $P_{\text{total loss}}$ representing the total power loss of elements.

3 Operation analysis in the DCM

DCM occurs when the value of the current through L_1 reaches zero before ending the first mode. In this case, there will be three operating modes. The first and third modes in the DCM are the same as the first and second modes in the CCM, respectively. The equivalent circuit of the second mode in the DCM is shown in Fig. 7 and the operating waveforms in the DCM are shown in Fig. 8.

Mode 1 in DCM [$t_0 \le t < t_1'$]: The duration of the first mode in the DCM will be equal to $D_x T$. The time duration of $D_x T$ is shown in Fig. 8. The operation of elements in this mode is the same as the first mode in the CCM. Thus, (1)–(3) are valid for the first operating mode in the DCM. The current ripple of L_1 in the DCM can be expressed as

$$\Delta I_{L1} = \frac{D_x(V_{\text{in}} + V_{C2} - V_{C3})}{L_1 f_s} \tag{26}$$

$$\begin{aligned} G_{\text{Real}} = {} & G_{\text{ideal}} - \left(\frac{1}{(1-3D)}\right) \\ & \times \left[I_{L1}\left[(2+2D)r_L + \frac{4 - 2(1-3D)(1-D)}{1-D} r_C + \frac{1-D}{D} r_S \right.\right. \\ & \left. + \frac{2 - (1-3D)(1-D)}{1-D} r_D \right] + V_{FD}(7 - 9D) \\ & \left. + I_{\text{in}}\left[\frac{3 - 7D + 4D^2}{1-D} r_D - 2Dr_S - 2D\right] + I_{\text{o}}\left[\frac{1-3D}{1-D} r_D - \frac{4D}{1-D} r_C\right] \right] \end{aligned} \tag{18}$$

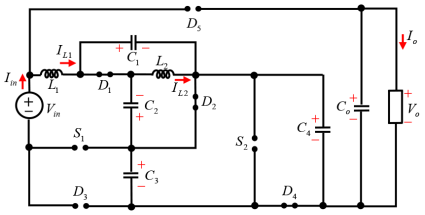

Fig. 7 *Equivalent circuit of the second mode in the DCM*

Mode 2 in DCM [$t_1' \le t < t_2'$]: In the second mode, I_{L1} reaches to zero, which leads to the reverse bias of D_3. Thus, S_1, S_2, D_3, and D_5 are off during this mode, while D_1, D_2, and D_4 are conducting. The following is valid:

$$v_{L1} = 0, I_{L1} = 0, v_{L2} = -V_{C2} = -V_{C1}, V_{C3} = V_{C4} \tag{27}$$

$$\begin{cases} v_{S1} = V_{\text{in}} + V_{C2}, v_{S2} = V_{C4} \\ V_{D3} = V_{\text{in}} + V_{C2} - V_{C3}, V_{D5} = V_o - V_{C4} + V_{C1} \end{cases} \tag{28}$$

Mode 3 in DCM [$t_2' \le t < t_2$]: The third operating mode in the DCM will be the same as the second mode in the CCM. Therefore, (4)–(6) are valid for this mode. The current ripple of L_1 in this mode is expressed as

$$\Delta I_{L1} = \frac{D(V_{\text{in}} + V_{C3} + V_{C1})}{L_1 f_s} \tag{29}$$

Applying the volt-second balance law for inductors leads to

$$\begin{cases} V_{C1} = \text{DV}_{C3}, V_{C3} = V_{C4} = 0.5(G_{\text{DCM}} - 1)V_{\text{in}} \\ V_{C1} = V_{C2} = 0.5D(G_{\text{DCM}} - 1)V_{\text{in}} \end{cases} \tag{30}$$

Considering (16) and (19) results in

$$D_x = \frac{D[V_{\text{in}} + (1+D)V_{C3}]}{[V_{C3}(1-D) - V_{\text{in}}]} \tag{31}$$

where D_x is shown in Fig. 8. The average value of I_{L1} in the DCM is obtained considering Fig. 8 as

$$I_{L1,\text{ave,DCM}} = 0.5\Delta I_{L1}(D + D_x) \tag{32}$$

In addition, (11) and (12) are valid in the DCM as

$$I_{L1,\text{ave,DCM}} = I_{L2,\text{ave,DCM}} = I_{\text{in}} - I_{\text{o}} = \frac{G_{\text{DCM}}(G_{\text{DCM}} - 1)V_{\text{in}}}{R} \tag{33}$$

The voltage gain in the DCM can be obtained considering (26), (29), and (31)–(33) as

$$G_{\text{DCM}} = \frac{3-D}{2(1-D)} + \frac{D^2(1+D)}{2(1-D)X} + \frac{\sqrt{[(D-3)X - D^2(1+D)]^2 + 4D^2(1-D)^2X}}{2(1-D)X} \tag{34}$$

where X is defined as $X = 2L_1/TR$. The critical value of X happens when the current flowing through L_1 is between the continuous and discontinuous modes. When considering $I_{L1,\text{ave,CCM}} = \Delta I_{L1}/2$, the critical X is as

$$X_{\text{Critical}} = \frac{D(1-3D)}{3} \tag{35}$$

According to (35), the converter operates in the DCM if $X_{\text{Critical}} < D(1–3D)/3$; otherwise, it operates in the CCM. The boundary

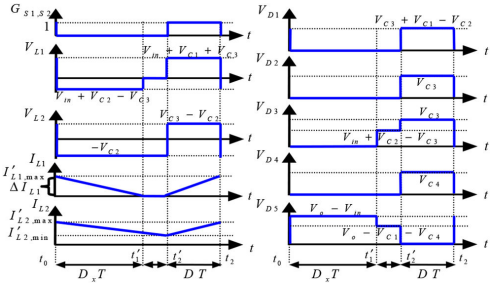

Fig. 8 *Steady-state waveforms of the proposed converter in the DCM*

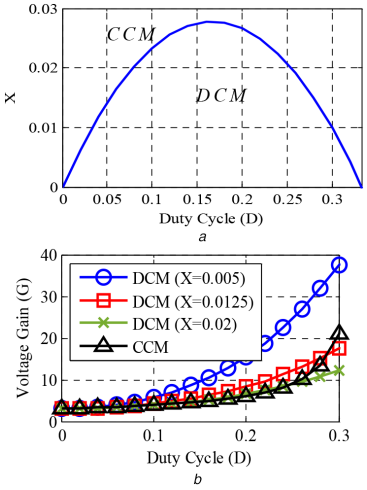

Fig. 9 *Voltage gains of the proposed converter*
(a) Boundary between the DCM and CCM, ***(b)*** Voltage gain of the proposed converter in the DCM and CCM

between the continuous and discontinuous modes is shown in Fig. 9*a*. Moreover, the voltage gains of the proposed converter in the CCM and DCM operations are also compared in Fig. 9*b*. As observed in Fig. 9, in general, the operation in the DCM will contribute to a large conversion gain.

4 Comparison with similar converters

To further demonstrate the features of the proposed converter, a comparison is done between the proposed DC–DC converter and the prior-art converters in Table 1. According to Table 1, the SC-SBC converter in [26] has the lowest total number of elements, while the presented converters in [22, 28, 29] with three qZS cells and the proposed extended converter have the highest total number of elements. Moreover, the type of the input current is continuous for the proposed converter and its extended topology. Only converters in [17, 29] represent the continuous input current. The converter in [22] has the widest duty cycle variation range and it will achieve its highest voltage gains in duty cycles close to one. In addition, the proposed extended topology shows the highest voltage gain in duty cycles lower than 0.22 and in duty cycles between 0.25 and 0.33. The comparison of voltage gains is shown in Fig. 10*a*. Fig. 10*b* presents the comparison of the normalised total voltage stress on capacitors versus the voltage gain. Based on Fig. 10*b*, the proposed converters in [26] have the lowest value for the total voltage stress on capacitors and the proposed extended converter has the second-lowest value. Fig. 10*c* demonstrates the comparison of the normalised total voltage stress on semiconductors. According to Fig. 10*c*, the converter in [29] with

Table 1 Comparison of the similar high step-up DC–DC converters

Parameters		Component number	switch	Voltage stress on diode	capacitor	Input current type	Duty cycle variation range	Voltage gain	Efficiency, %
Fig. 1		2*S*, 5*D*, 2*L*, 5*C* 2*S*	$\frac{GV_{in}}{3(1-D)}$	$\frac{GV_{in}}{3(1-D)}$, $(G-1)V_{in}$	$\frac{DGV_{in}}{3(1-D)}$, $\frac{GV_{in}}{3(1-D)}$	cont.	$0 < D \leq 0.33$	$\frac{3(1-D)}{1-3D}$	98
Fig. 4		2*S*, 6*D*, 2*L*, 6*C*	$\frac{GV_{in}}{3(1-D)}$	$\frac{GV_{in}}{3(1-D)}$, $(G-1)V_{in}$, $\frac{2}{3}GV_{in}$	$\frac{DGV_{in}}{3}$, $\frac{GV_{in}}{3}$, DGV_{in}	cont.	$0 < D \leq 0.33$	$\frac{3}{1-3D}$	96
[29]	two qZS cells	1*S*, 3*D*, 3*L*, 5*C*	GV_{in}	GV_{in}	DGV_{in}, $2DGV_{in}$ $(1-2D)GV_{in}$	cont.	$0 < D \leq 0.33$	$\frac{1}{1-3D}$	97
	three qZS cells	1*S*, 4*D*, 4*L*, 7*C*	GV_{in}	GV_{in}	$(1-2D)GV_{in}$, DGV_{in} $(1-3D)GV_{in}$, $2DGV_{in}$	cont.	$0 < D \leq 0.33$	$\frac{1}{1-4D}$	98
[28]		1*S*, 5*D*, 3*L*, 7*C*	$\frac{GV_{in}}{2+D}$	$\frac{GV_{in}}{2+D}$	$\frac{D}{2+D}GV_{in}$, $\frac{1}{2+D}GV_{in}$ $\frac{2D}{2+D}GV_{in}$, $\frac{1-D}{2+D}GV_{in}$	cont.	$0 < D < 0.25$	$\frac{2+D}{1-2D}$	94
[26]	SL/SC-SBC	2*S*, 7*D*, 2*L*, 3*C*	$\frac{DGV_{in}}{1-D}$, $\frac{GV_{in}}{2}$	$\frac{DGV_{in}}{1-D}$, $\frac{GV_{in}}{2}$, $\frac{DGV_{in}}{2(1-D)}$	$\frac{DGV_{in}}{1-D}$, $\frac{GV_{in}}{2}$	discont.	$0 < D \leq 0.33$	$\frac{2(1-D)}{1-3D}$	95
	SC-SBC	2*S*, 4*D*, 1*L*, 3*C*	$\frac{GV_{in}}{2}$, $\frac{DGV_{in}}{2(1-D)}$	$\frac{GV_{in}}{2+D}$, $\frac{(1-D)GV_{in}}{2}$	$\frac{GV_{in}}{2}$, $\frac{DGV_{in}}{2(1-D)}$	discont.	$0 < D < 0.5$	$\frac{2(1-D)}{1-2D}$	94
[22]		2*S*, 5*D*, 3*L*, 6*C*	$\frac{GV_{in}}{2+D}$, $\frac{(1-D)GV_{in}}{(2+D)}$	$\frac{GV_{in}}{1-D}$, $\frac{GV_{in}}{2}$	$\frac{GV_{in}}{2+D}$, $\frac{DGV_{in}}{2+D}$, $\frac{(1-D)GV_{in}}{2+D}$	discont.	$0 < D < 1$	$\frac{2+D}{(1-D)^2}$	95
[17]		1*S*, 3*D*, 4*L*, 4*C*	GV_{in}	$\frac{GV_{in}}{1-D}$, $\frac{GV_{in}}{2}$	$\frac{GV_{in}}{2}$, $\frac{(1+D)GV_{in}}{2(1-D)}$	cont.	$0 < D \leq 0.33$	$\frac{2(1-D)}{1-3D}$	91

three qZS cells has the highest total voltage stress on its semiconductors and the proposed extended converter has the second-highest value. Moreover, the proposed converter is shown in Fig. 1 and the converter presented in [29] with three qZS cells have the highest efficiency in the almost same condition (the input voltage of 40 V, the output power of 140 W, the output resistance of 400 Ω). Note that efficiencies of converters in Table 1 are extracted from the data and diagrams exist in references with an acceptable approximation.

5 Simulation and experimental results

5.1 Simulation

A simulation is done utilising the values of Table 2 for the CCM and Table 3 for the DCM to validate the theoretical analysis. Simulation results of the proposed converter (Fig. 1) in the CCM and DCM are shown in Figs. 11 and 12, respectively. Based on Fig. 11*a*, the proposed converter gives $V_o = 240$ V for the input voltage equal to 40 V. The obtained simulation value for the output voltage is compatible with the theoretical value from (4) with the value of 240 V. Fig. 11*b* gives $V_{C1} = 20$ V and $V_{C3} = 100$ V. The waveforms of V_{C2} and V_{C4} are similar to V_{C1} and V_{C3}. Thus, they have not been shown in Fig. 11. Theoretical values for V_{C1} and V_{C3} are 20 and 100 V based on (7). Fig. 11*c* shows the voltage waveforms of inductors with values of $V_{L1,max} = 160$ V, $V_{L1,min} = -40$ V, $V_{L2,max} = 80$ V and $V_{L2,min} = -20$ V. These values are the same as theoretical values obtained from (1) and (4). Fig. 11*d* shows the currents flowing through inductors with average values of $I_{L1,ave} = I_{L2,ave} = 2.95$ A and current ripples of $\Delta I_{L1} = 2\Delta I_{L2} = 0.5$ A. According to (9)–(12), the theoretical values for inductors currents are $I_{L1,ave} = I_{L2,ave} = 3$ A and $\Delta I_{L1} = 2\Delta I_{L2} = 0.5$ A. Fig. 11*e* shows the voltage and current waveforms of the switch S_1 with the voltage stress equal to 100 V. Fig. 11*f* gives the voltage and current waveforms of the diode D_5 with the voltage stress equal to 200 V. The voltage stress of the switch S_2 and diodes D_1, D_2, D_3, and D_4 are equal to the voltage stress of the switch S_1.

Fig. 12 shows the simulation results of the proposed converter in the DCM using values of Table 3. Fig. 12*a* presents $V_o = 239$ V for the input voltage of 30 V. The theoretical output voltage obtained from (34) is $V_o = 242.4$ V. Fig. 12*b* presents $V_{C1} = 20.7$ V and $V_{C3} = 104$ V. The theoretical values obtained from (30) are equal to $V_{C1} = 21$ V and $V_{C3} = 105$ V. Fig. 12*c* gives the voltage waveforms of inductors with values of $V_{L1,max} = 154$ V, $V_{L1,min} = -53$ V, $V_{L2,max} = 83$ V and $V_{L2,min} = -20.7$ V. The voltage across the inductor L_1 is zero during the second mode in the DCM. Fig. 12*d* shows the current of the inductor L_1 that is discontinuous. Figs. 12*e* and *f* show the voltage and current waveforms of the switch S_1 and the diode D_5, respectively. The voltage stress of S_1 is 104 V, while the voltage stress of D_5 is equal to 208 V. In addition, during the second mode in the DCM, the voltages across S_1 and D_5 are 50.7 and 154 V, respectively. The theoretical values in the second mode in the DCM based on (28) are $V_{S1} = 105$ V and $V_{D5} = 209$ V.

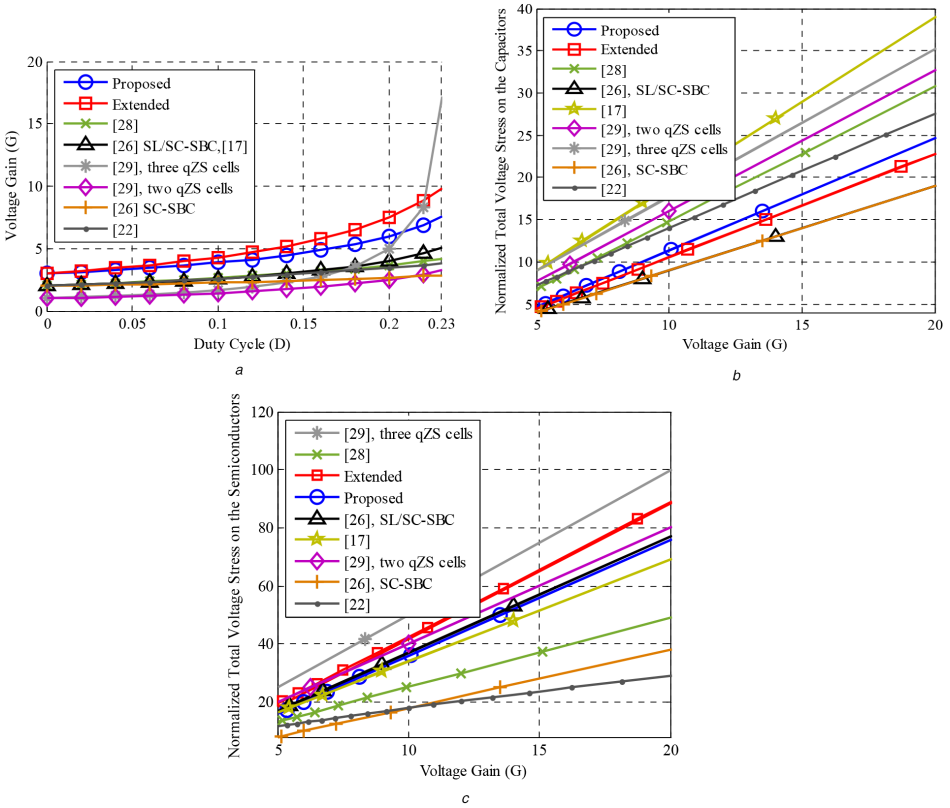

Fig. 10 *Comparison of the parameters for the converters presented in Table 1*
(a) Voltage gain comparison, ***(b)*** Normalised total voltage stress on capacitors versus the voltage gain, ***(c)*** Normalised total voltage stress on semiconductors versus the voltage gain

Table 2 Values of the components used in simulation

Parameter	Value	Parameter	Value
V_{in}	40 V	L_1&L_2	640 μH
$C_1, \ldots, C_5$	100 μF	D	0.2
f_S	100 kHZ	R	400 Ω
G	6	P_o	144 W

Table 3 Values of the components used in simulation and Experimental for the DCM

Parameter	Value	Parameter	Value
V_{in}	30 V	L_1	28.8 μH
$C_1, \ldots, C_5$	100 μF	L_2	640 μH
f_S	100 kHZ	D	0.2
G	8.08	R	400 Ω

Finally, Fig. 13 shows the simulation results of the extended proposed converter (Fig. 4) based on values in Table 2. Fig. 13*a* gives $V_o = 300$ V for the input voltage of 40 V. The theoretical value for the output voltage based on (8) and parameters in Table 2 is 300 V. Fig. 13*b* presents $V_{C1} = 20$ V, $V_{C3} = 100$ V, $V_{C5} = 60$ V, which are the same as theoretical values in (8). Moreover, Figs. 13*c* and *d* show the voltage and current of the switch S_1 and the diode D_6 with voltage stress of 100 and 200 V, respectively. As shown, the voltage stress on devices and capacitors are not changed in the extended topology compared to the main proposed converter in Fig. 1, but the voltage gain has been extended.

5.2 Experimental tests

To verify the theoretical and simulation values, an experimental setup is built and shown in Fig. 14. The experimental results of the proposed converter in the CCM are only shown in Fig. 15 based on the values in Table 2. According to Fig. 15*a*, $V_{C1} = 20$ V and $V_{C3} = 99$ V. The voltage waveforms of C_2 and C_4 are not shown due to their similarity to C_1 and C_3. In addition, Fig. 15*b* gives $V_{S1,max} = 99$ V and $I_{L1,ave} = 2.96$ A. Fig. 15*c* shows the waveform of the voltage across S_2 with the maximum voltage of 99 V. The voltage stress of the diodes D_1, D_2, D_3 and D_4 are the same as the switch S_1

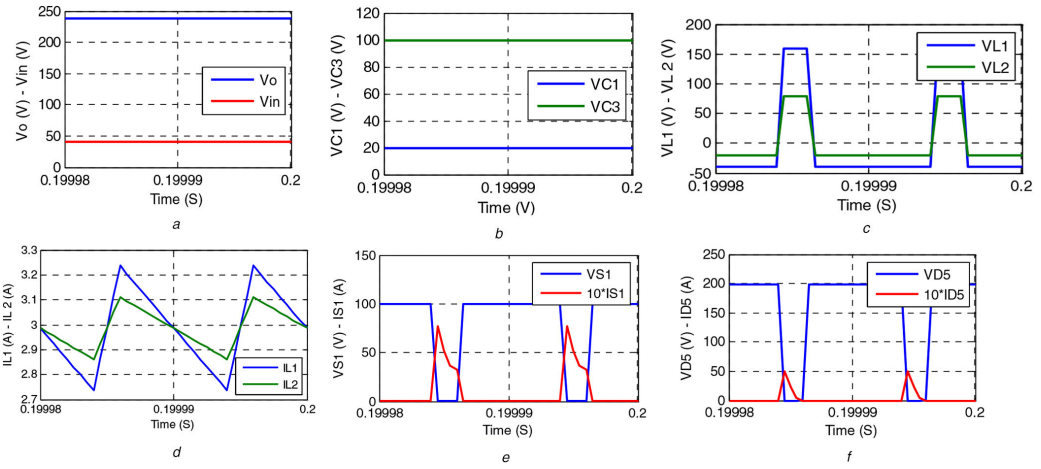

Fig. 11 *Simulation results of the proposed DC–DC converter operating in the CCM*

(a) Input and output voltages, ***(b)*** Voltages across the capacitors C_1 and C_3, ***(c)*** Voltages across the inductors, ***(d)*** Currents flowing through the inductors, ***(e)*** Voltage and current waveform of the switch S_1, ***(f)*** Voltage and current waveform of the diode D_5

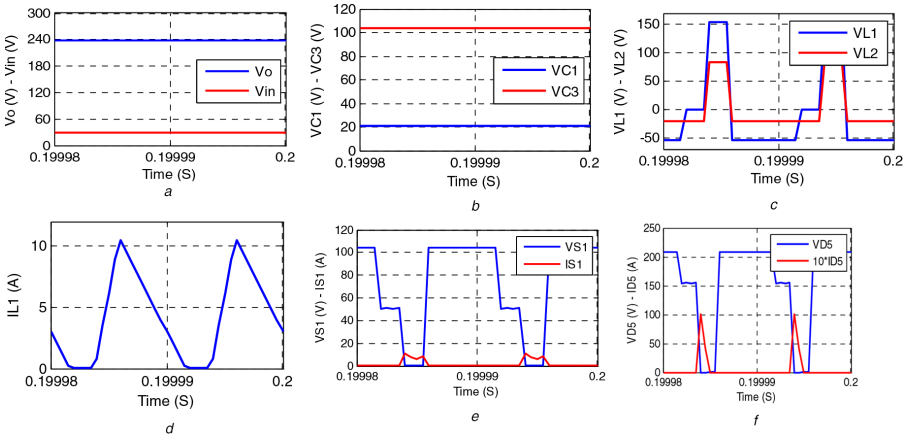

Fig. 12 *Simulation results of the proposed DC–DC converter operating in the DCM*

(a) Input and output voltages, ***(b)*** Voltages across the capacitors C_1 and C_3, ***(c)*** Voltages across the inductors, ***(d)*** Current flowing through the inductor L_1, ***(e)*** Voltage and current waveform of the switch S_1, ***(f)*** Voltage and current waveform of the diode D_5

and they are not shown to avoid repetition. Finally, Fig. 15*d* gives $V_o = 238$ V, $I_{L1} = 2.96$ A, $I_{L2} = 2.89$ A and $\Delta I_{L1} = 2\Delta I_{L2} = 0.5$ A. These results are obtained in the output power of 141 W and the voltage gain of 5.95. In addition, the experimental efficiency of the proposed converter is 98% for the output power of 141 W. The simulation and experimental efficiencies are almost the same since the internal resistance of elements has been considered in the simulation. Moreover, the output power of the experimental setup is low (141 W) and in low output powers, the conduction loss of the converter is low due to the low duty cycles. For higher powers, the efficiency difference between simulations and experiments will become larger due to higher thermal resistance in the experimental setup. The comparison between the experimental and theoretical values is shown in Table 4 and Fig. 16 compares the theoretical and experimental voltage gains for the proposed converter. It is concluded that the experimental and theoretical values match well.

The power density of the converter, ρ, can be obtained by dividing the output power over the volume of the converter as

$$\rho = \frac{P_o}{\text{Volume}} = \frac{141}{173.74 = 0.81(\text{W/cm}^3)} \tag{36}$$

Note that the optimisation in the power density for the proposed converter is not the primary purpose of this paper. More desirable power densities can be obtained by better selection and replacement of the elements in the experimental setup, which will be future work.

Finally, the experimental results of the proposed converter in the DCM using values of Table 3 are shown in Fig. 17. Based on Fig. 17*a*, the output voltage is 234.5 V, the average current flowing through L_1 is 4.27 A, and the average current flowing through L_2 is 4.18 A. Fig. 17*b* gives the voltage stress of the switch S_1 with the value of 102 V. In addition, the discontinuous conduction of the inductor L_1 is shown in Fig. 17*b*. The experimental values in the DCM are compatible with simulation and theoretical values.

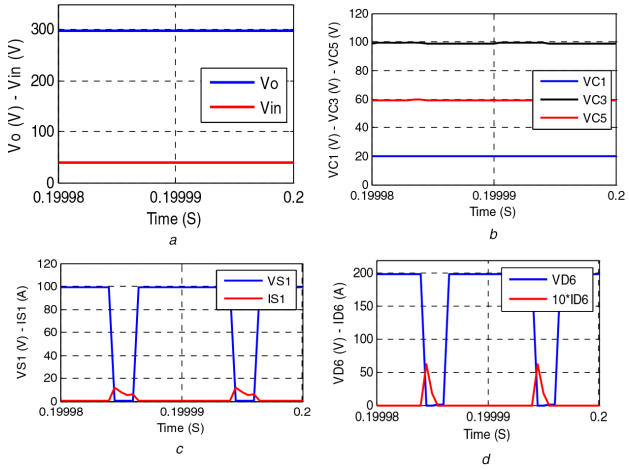

Fig. 13 *Simulation results of the proposed extended converter*
(a) Input and output voltages, ***(b)*** Voltages across the capacitors, ***(c)*** Voltage and current waveform of the switch S_1, ***(d)*** Voltage and current waveform of the diode D_6

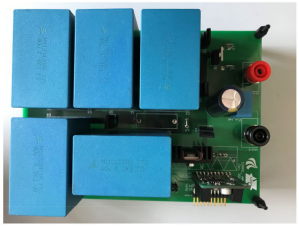

Fig. 14 *Experimental setup of the proposed converter*

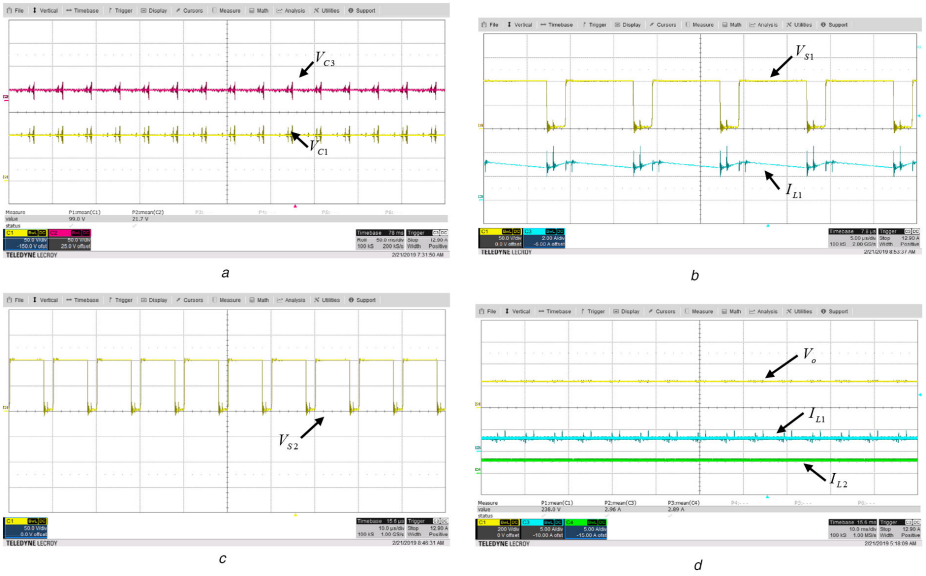

Fig. 15 *Experimental results of the proposed converter in the CCM*
(a) Capacitor voltages V_{C1} [50 V/div] and V_{C3} [50 V/div], ***(b)*** Voltage across the switch V_{S1} [50 V/div] and the inductor current I_{L1} [2 A/div], ***(c)*** Voltage across the switch V_{S2} [50 V/div], ***(d)*** Output voltage V_o [200 V/div] and inductors currents I_{L1} [5 A/div] and I_{L2} [5 A/div]

Table 4 Comparison between the experimental and theoretical values

Experimental	Theoretical	Experimental	Theoretical
$V_o = 238$ V	$V_o = 240$ V	$I_{L1} = 2.96$ A	$I_{L1} = 3$ A
$V_{C1} = 20$ V	$V_{C1} = 20$ V	$I_{L2} = 2.89$ A	$I_{L2} = 3$ A
$V_{C3} = 99$ V	$V_{C3} = 100$ V	$\Delta I_{L1} = 0.5$ A	$\Delta I_{L1} = 0.5$ A
$G = 5.95$	$G = 6$	$\Delta I_{L2} = 0.25$ A	$\Delta I_{L2} = 0.25$ A
$P_o = 141$ W	$P_o = 144$ W	$V_{S1,max} = 99$ V	$V_{S1,max} = 100$ V

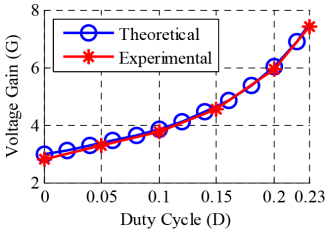

Fig. 16 *Comparison of the theoretical and experimental voltage gains*

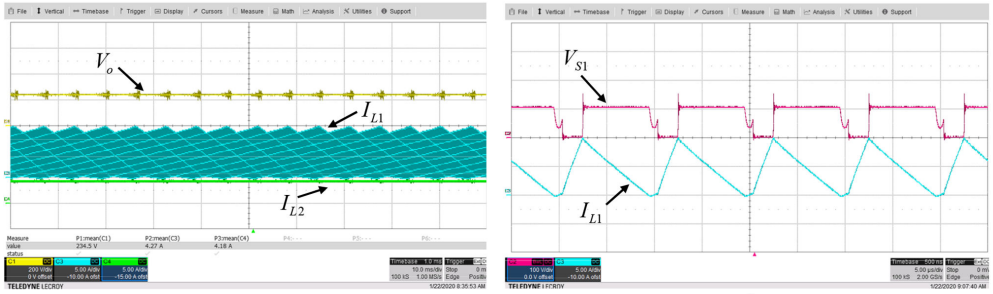

Fig. 17 *Experimental results of the proposed converter in the DCM*

(a) The output voltage V_O [200 V/div], and the inductors currents I_{L1} and I_{L2} [5 A/div], ***(b)*** The voltage across the switch V_{S1} [100 V/div] and the inductor current I_{L1} [5 A/div]

6 Conclusion

In this paper, a modified high voltage-gain qZS DC–DC converter adopting an SC network was proposed. The proposed converter can achieve high voltage gains in low duty cycles and low voltage stress on its elements. In this paper, the steady-state analysis in the DCM and CCM along with the design procedure was prepared. Then, the calculation of the non-ideal voltage gain, the power loss analysis and an extended topology were given. The comparison with the prior-art converters highlighted the advantages and drawbacks of the proposed converter. Finally, the simulation and experimental results verified the theoretical analysis.

7 References

[1] Guo, F., Fu, L., Zhang, X., *et al.*: 'A family of quasi-switched-capacitor circuit based dual-input DC/DC converters for photovoltaic systems integrated with battery energy storage', *IEEE Trans. Power Electron.*, 2016, **31**, (12), pp. 8237–8248

[2] Ahrabi, R.R., Ardi, H., Elmi, M.: 'A novel step-up multi-input DC-DC converter for hybrid electric vehicles application', *IEEE Trans. Power Electron*, 2017, **32**, (5), pp. 3549–3561

[3] Meinagh, F.A.A., Babaei, E., Tarzamni, H., *et al.*: 'Isolated high step-up switched-boost DC/DC converter with modified control method', *IET Power. Electron.*, 2019, **12**, (14), pp. 3635–3645

[4] Meinagh, F.A.A., Ranjbarizad, V., Babaei, E.: 'New non-isolated high voltage gain single-switch DC-DC converter based on voltage-lift technique'. Proc. PEDSTC, Shiraz, Iran, 2019, pp. 219–223

[5] Yang, J., He, Z., Pang, H., *et al.*: 'The hybrid-cascaded DC-DC converters suitable for HVDC applications', *IEEE Trans. Power Electron.*, 2015, **30**, (10), pp. 5358–5363

[6] Shahir, F.M., Babaei, E., Farsadi, M.: 'Voltage-lift technique based non-isolated boost DC-DC converter: analysis and design', *IEEE Trans. Power. Electron.*, 2018, **33**, (7), pp. 5917–5926

[7] Kawa, A., Stala, R., Mondzik, A., *et al.*: 'High-power thyristor-based DC-DC switched-capacitor voltage multipliers: basic concept and novel derived topology with reduced number of switches', *IEEE Trans. Power Electron.*, 2016, **31**, (10), pp. 6797–6813

[8] Salvador, M.A., Lazzarin, T.B., Coelho, R.F.: 'High step-up DC-DC converter with active switched-inductor and passive switched-capacitor networks', *IEEE Trans. Ind. Electron.*, 2018, **65**, (7), pp. 5644–5654

[9] Andrade, A.M.S.S., Mattos, E., Schuch, L., *et al.*: 'Synthesis and comparative analysis of very high step-Up DC-DC converters adopting coupled-inductor and voltage multiplier cells', *IEEE Trans. Power Electron.*, 2018, **33**, (7), pp. 5880–5897

[10] Peng, F.Z.: 'Z-source inverter', *IEEE Trans. Ind. Appl.*, 2003, **39**, (2), pp. 504–510

[11] Vinnikov, D., Roasto, I.: 'Quasi-Z-source based dc/dc converters for distributed power generation', *IEEE Trans. Ind. Electron.*, 2011, **58**, (1), pp. 192–201

[12] Meinagh, F.A.A., Babaei, E., Tarzamni, H.: 'Modified high voltage gain switched boost inverter', *IET Power Electron.*, 2017, **10**, (13), pp. 1655–1664

[13] Meinagh, F.A.A., Babaei, E., Vinnikov, D., *et al.*: 'Modified high voltage gain soft-switched quasi-switched boost inverter'. Proc. ICIT, Melbourne, Australia, 2019, pp. 1087–1092

[14] Siwakoti, Y.P., Blaabjerg, F.: 'Single switch nonisolated ultra-step-Up DC–DC converter with an integrated coupled inductor for high boost applications', *IEEE Trans. Power. Electron.*, 2017, **32**, (11), pp. 8544–8558

[15] Forouzesh, M., Shen, Y., Yari, K., *et al.*: 'High-efficiency high step-up DC-DC converter with dual coupled inductors for grid-connected photovoltaic systems', *IEEE Trans. Power Electron.*, 2018, **33**, (7), pp. 5967–5982

[16] Das, M., Agarwal, V.: 'Generalized small signal modeling of coupled-inductor-based high-gain high-efficiency DC-DC converters', *IEEE Trans. Ind. App.*, 2017, **53**, (3), pp. 2257–2270

[17] Takiguchi, T., Koizumi, H.: 'Quasi-Z-source dc-dc converter with voltage-lift technique'. Proc. IECON, Vienna, Austria, 2013, pp. 1191–1196

[18] Vinnikov, D., Roasto, I., Strzelecki, R., *et al.*: 'Step-up dc/dc converters with cascaded quasi-Z-source network', *IEEE Trans. Ind. Electron.*, 2012, **59**, (10), pp. 3727–3736

[19] Chen, Z., Chen, Y., Jiang, C., *et al.*: 'A quasi-Z source network with multiple switch-inductor cells and Cockroft-Walton voltage multipliers'. Proc. IECON, Beijing, People's Republic of China, 2017, pp. 8009–8014
[20] Nguyen, M., Lim, Y., Cho, G.: 'Switched-inductor quasi-Z-source inverter', *IEEE Trans. Power. Electron.*, 2011, **26**, (11), pp. 3183–3191
[21] Raveendran, A., Paul, E., Ommen, A. P.: 'Quasi-Z-source dc-dc converter with switched capacitor', *Int. J. Eng. Res.Gen. Sci.*, 2015, **3**, (4), pp. 1132–1137
[22] Jalilzadeh, T., Rostami, N., Babaei, E., *et al.*: 'Non-isolated topology for high step-up DC-DC converters', *IEEE Emerg. Select. Topics Power Electron.*, 2018, doi: 10.1109/JESTPE.2018.2849096, to appear
[23] Shen, H., Zhang, B., Qiu, D., *et al.*: 'A common grounded Z-source dc–dc converter with high voltage gain', *IEEE Trans. Ind. Electron.*, 2016, **63**, (5), pp. 2925–2935
[24] Patidar, K., Umarikar, A. C.: 'High step-up pulse-width modulation DC–DC converter based on quasi-Z-source topology', *IET Power. Electron.*, 2015, **8**, (4), pp. 477–488
[25] Karthikeyan, V., Kumaravel, S., Kumar, G.G.: 'High step-up gain DC-DC converter with switched capacitor and regenerative boost configuration for solar PV applications', *IEEE Trans. Circuit. System II*, 2019, **66**, (12), pp. 2022–2026
[26] Zhu, X., Zhang, B., Li, Z., *et al.*: 'Extended switched-boost DC-DC converters adopting switched-capacitor/switched-inductor cells for high step-up conversion', *IEEE J. Emerg. Select. Top. Power Electron*, 2017, **5**, (3), pp. 1020–1030
[27] Zhang, Y., Fu, C, Sumner, M., *et al.*: 'A wide input-voltage range quasi-Z source boost DC-DC converter with high voltage-gain for fuel cell vehicles', *IEEE Trans. Ind. Electron*, 2018, **65**, (6), pp. 5201–5212
[28] Haji-Esmaeili, M.M., Babaei, E., Sabahi, M.: 'High step-Up quasi-Z source DC-DC converter', *IEEE Trans. Power. Electron.*, 2018, **33**, (12), pp. 10563–10571
[29] Shen, H., Zhang, B., Qiu, D.: 'Hybrid Z-source boost DC-DC converters', *IEEE Trans. Ind. Electron.*, 2017, **64**, (1), pp. 310–319
[30] Meinagh, F.A.A., Yuan, J., Yang, Y.: 'New high voltage gain DC-DC converter based on modified quasi Z-source network'. Proc. CPE-POWERENG., Sonderborg, Denmark, 2019, in press

Conference publication 1

An Overview of Photovoltaic Microinverters: Topology, Efficiency, and Reliability

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An Overview of Photovoltaic Microinverters: Topology, Efficiency, and Reliability

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***Abstract*—This paper presents an overview of microinverters used in photovoltaic (PV) applications. Conventional PV string inverters cannot effectively track the optimum maximum power point (MPP) of the PV string due to the series configuration (especially, under partial shading conditions). In order to tackle this problem, microinverters make each PV panel operate at its own MPP so that the overall efficiency can be improved. In this paper, a detailed analysis is carried out among commercially-available microinverters in terms of topological structure and operational principle. Moreover, the latest products on the microinverter market and future trends of the microinverters are discussed in terms of efficiency and reliability.**

***Index Terms*—microinverter, PV application, flyback converter, DC-DC inverter, DC-AC inverter**

I. Introduction

Renewable energy systems have experienced a rapid development in last decades and the penetration level is still increasing due to the demand to reduce the fossil fuel consumption globally. Especially, the share of the solar PV capacity in newly installed renewable energy capacity was around 55% in 2017 [2]. In order to harvest the solar energy, a PV inverter is essential to transfer the PV energy to the utility grid or load. Generally, the grid-connected inverters in PV systems can be classified into central inverters, string inverters and AC-module converters, also known as named microinverters [3].

In the traditional PV applications with central or string inverters, all the PV modules are controlled by a power converter. In this case, the overall performance of the system can be degraded significantly if one module in the shaded or faulty state. That is, the inverter cannot achieve the maximum power point tracking (MPPT) of each PV modules due to the series configuration. Moreover, the series connection of PV modules has a limited fault tolerance capability as the failure of one single PV module can cause the loss of power production of the entire PV string. To address this, the microinverter concept was introduced and it features low installation and maintenance costs, 'plug-and-play' operation, modularity and high efficient systems [4], [5]. In this configuration, each PV module is individually connected to a microinverter, and thus, the overall system efficiency and reliability may be improved by achieving the individual MPPT operation and eliminating the potential faulty condition [6], in particular, under partial shading conditions, the microinverters especially suitable for small-scale residential or commercial applications [7].

In general, the microinverter can be divided into two categories–single-stage and two-stage PV microinverter configurations. The single-stage microinverter is normally operated with the functions of boosting capability, MPPT, grid current control in single power conversion [8], [9]. As a relatively low voltage from the PV module should be boosted, the flyback converter is widely adopted in PV microinverters. For instance, as shown in Fig. 1, a single-stage microinverter is depicted, which includes a flyback inverter and a full-bridge unfolder to obtain the full sinusoid [1]. The main disadvantage of such a single-stage microinverter is that the double-line-frequency voltage ripples must be filtered at the PV-side. This requires large electrolytic capacitors (C_{pv}) at the PV side, which may be prone to failure under extreme conditions, e.g., high temperature [10]. Alternatively, the two-stage microinverters were developed in the literature, where the double-line-frequency voltage ripples can be buffered in the DC-link capacitor [11]. A two-stage microinverter has a step-up DC/DC inverter and a DC/AC converter to achieve the power injection. Although the two-stage microinverter can be separately optimized, the overall efficiency is decreasing due to the losses in both stages and the system cost is higher because of the high component count.

Recently, many efforts have been made to improve the performance of microinverters through topological innovations. Among others, the flyback-based microinverter, as shown in Fig. 1, is still one of the most widely used topologies as a single-stage configuration due to its simple control, low component counts and inherent galvanic isolation [12], [13]. Many attempts have also been made to improve the performance of the flyback microinverter by modifying the topology. For example, in order to recycle the leakage energy and achieve soft switching for the primary side active power devices, an active-clamped flyback converter with an unfolder was proposed in [12], as shown in Fig. 2. For two-stage topologies, the interleaved flyback converter and interleaved isolated boost converter are promising candidates as in the DC-DC stage [14], [15]. Furthermore impedance source networks [16], [17] can also be adopted in microinverters. This is promising due to the attractive feature that the input voltage can be boosted during the shoot-through state. In [18] and [19], a high-performance quasi-Z-source series-resonant dc-dc converter was proposed as a promising topology for PV microinverters, which provides a wide input voltage and load regulation range thanks to the multi-mode operation.

Commercial products are also available on the market based on the above topologies. The M250 microinverter is a repre-

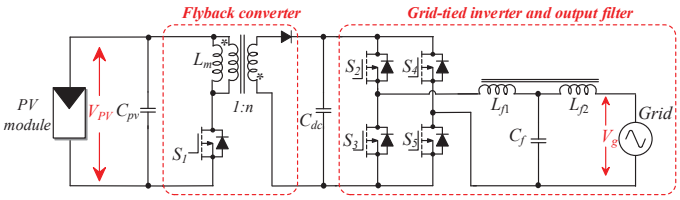

Fig. 1. Single-stage flyback microinverter [1], where L_m is the leakage inductance.

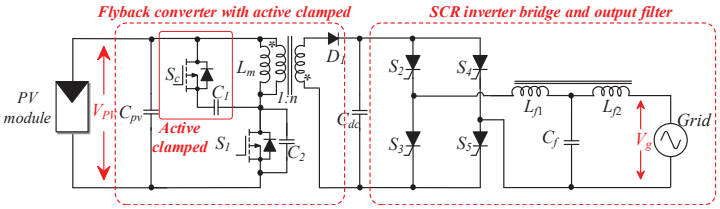

Fig. 2. Single-stage flyback microinverter with an active clamp circuit (SCR – Silicon-Controlled Rectifier) [12]

sentative product from Enphase Energy, which is based on the topology shown Fig. 1 [10]. In the past two years, Enphase has released the latest generation microinverter, Enphase IQ 7/7+ microinverter, which provides higher efficiency compared with the previous products [20]. Moreover, Texas Instruments (TI) also developed a two-stage PV microinverter using an active clamp flyback DC/DC converter with a secondary voltage multiplier and a DC/AC inverter [21]. In addition, ST Microelectronics launched a 250-W grid-connected microinverter [15], where an interleaved isolated DC/DC converter was employed.

Although certain microinverters have been extensively discussed in the literature, it still lacks a general benchmarking for the commercial microinverter products. In this paper, the operation principles of the representative microinverter products for PV applications are presented in detail. Moreover, a detailed comparison among these products is discussed in terms of power rating, total harmonic distortion (THD), efficiency and reliability. Finally, it outlines the future directions to improve the performance of PV microinverters.

II. Operation Principles of the Selected Products

A. Single-stage PV microinverter

As shown in Fig. 3, the single-stage microinverter consists of two interleaved quasi-resonant flyback converter and a full-bridge unfolder. As discussed previously, the commercial product M250 from Enphase Energy is designed based on the topology shown in Fig. 1. Notably, it is a interleaved network which consists two flyback converters in parallel to meet the power requirements.

The flyback converter can be treated as a combination of a buck-boost converter and a high-frequency (HF) transformer with the turns-ratio being $1/n$. According to Fig. 1, when S_1 is ON, the primary side inductor is charged by the PV module, and the inductor current increases linearly. When S_1 is turned OFF, the stored energy in the primary-side inductor is delivered to grid/load side through the secondary side inductor. It should be noted that, normally, this system operates in the discontinuous conduction mode (DCM), where the losses can be reduced compared with the continuous conduction mode (CCM). Moreover, for the single-stage microinverter, the output voltage of the flyback converter is a rectified sinusoidal wave, which is also named a pseudo DC-link. The full-bridge inverter is then used to unfold the rectified voltage into a full sinusoidal voltage [22], [23].

B. Two-stage PV microinverter

For two-stage PV microinverter products, they can be classified as flyback-based, isolated-boost-based and impedance-source based converters. Compared with the single-stage mi-

Fig. 3. Photo of the Enphase microinverter M250 [10].

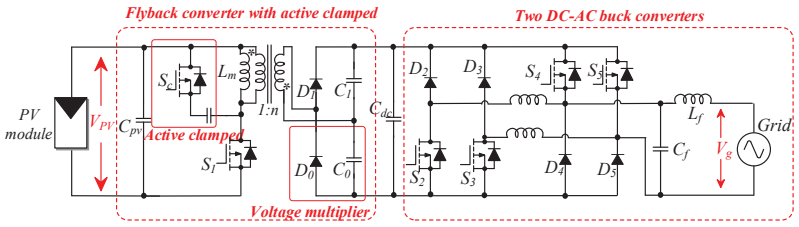

Fig. 4. TI's microinverter topology [21].

Fig. 5. Photo of TI's microinverter [21].

croinverter, it is clear that two-stage microinverter requires two power conversion stages, i.e., DC/DC and DC/AC. The DC/DC converter is used to achieve the MPPT and the DC/AC converter is used to convert the extracted DC power into the AC power and deliver it to the grid. The TI 280-W microinverter, as shown in Figs. 4 and 5, is based on an active-clamped interleaved flyback converter and a HF inverter. Compared with the converter in Fig. 1, the difference is that this DC-AC inverter operates at a high frequency while the converter in Fig. 1 only operates at the grid frequency (i.e., unfolding stage).

The operation principle of the TI's product can be summarized as following. First, the DC-DC active-clamped flyback converter draws the DC current from the PV panel and achieves the MPPT. Moreover, this flyback converter provides an HF isolation and the output voltage of the flyback converter is a high voltage. The inverter is then controlled to inject the expected current into the grid.

The 250-W microinverter from ST Microelectronics is shown in Figs. 6 and 7, and it is based on two power conversion stages: an interleaved isolated boost DC-DC converter and a mixed frequency DC-AC converter [15]. The isolated boost converter has four operation modes. First, the switches $S_1$and S_2 are turned ON and the current flows through the inductors. In the second mode, the switch S_1 is still ON but S_2 is turned OFF. Then the stored energy in L_2 is delivered to the secondary side so that the capacitor C_2 is charged. The third mode is the same as the first one. The last mode is contrary to the second mode, where S_1 is OFF and S_2 is turned ON, so the energy stored in L_1 is delivered to the secondary side. The DC-AC converter employs a hybrid modulation technique, where the power switches S_3 and S_4 operate at a high switching frequency, while the switches S_5 and S_6 only operate at the grid frequency. Moreover, the diodes D_3 and D_4 are used to inhibit the internal body diode, and the diodes D_5 and D_6 is used to overcome the potential problems when the MOSFET S_3 and S_4 turn on.

Figs. 8 and 9 show a quasi-Z-source (qZS)-based microinverter topology [18], [24] and its microinverter product is released as UBIK S350 OPTIVERTER. The qZS-microinverter includes a synchronous qZS network, a full-bridge inverter, a hybrid transformer with resonant inductors, a voltage doubler rectifier and a grid-tie inverter. This topology has the following features:

1) Compared with the traditional qZS inverter [25], the original input diode is replaced by a n-channel MOSFET, which can reduce the conduction losses.
2) A coupled inductor is implemented to replace the two discrete inductors in the traditional qZS network [25], which improves the power density and reduces the input current ripples.
3) External resonant tanks are not needed due to the fully integrated series-resonant tank, which lowers the volume and cost of the converter.

The operation of this topology can be divided into three modes: 1) normal mode, 2) buck mode, and 3) boost mode. In the normal mode, the MPP voltage of the PV module equals to the expected operating voltage and the operation principle in this mode is similar to that of conventional series-resonant converter at the resonant frequency. When the PV input voltage is higher than the expected, the converter operates in the buck mode. In this mode, the phase-shift modulation technique is used to control the output voltage. If the input voltage from the PV module is lower than the predefined value, this topology operates in the boost mode like a traditional qZS inverter and the boosted voltage can be obtained by increasing the shoot-through duty ratio.

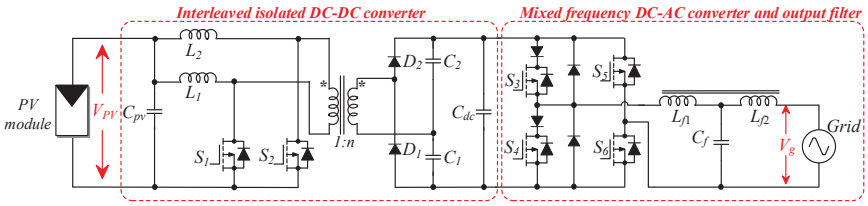

Fig. 6. The microinverter topology from ST Microelectronics [15].

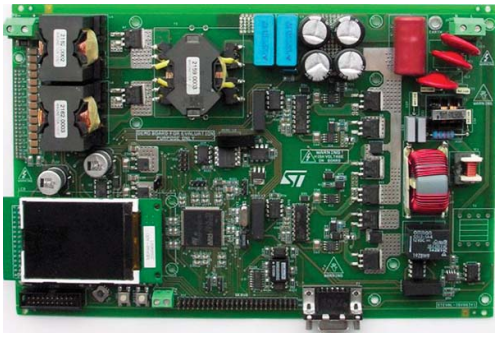

Fig. 7. Photo of the microinverter from ST Microelectronics [15].

III. Comparison and Analysis of the Selected Microinverters

In order to benchmark the above four microinverters, a detailed comparison among these four topologies is carried out.The comparison of the above four topologies is summarized in Table I, where CEC stands for California Energy Commission.

Clearly, the selected four products are isolated PV microinverters, which can provide a galvanic isolation and a high voltage gain compared with non-isolated solutions. As it can be seen from Table I, the selected products power ratings from 250 W to 300 W. Moreover, it is observed that the Enphase M250 as a single-stage solution has the lowest total component count, which can lead to cost-saving. However, the main drawback of the M250, like most of the single-stage microinverters, is that a very large electrolytic decoupling capacitor is needed in order to filter out the double-line- frequency voltage ripples, as mentioned in Section I.

When only considering the number of active switches, it is interesting that although Enphase, TI and ST products have the same number of active switches, the power devices of the Enphase microinverter operating at a low frequency are more than the other products. Therefore, the efficiency and reliability of the Enphase converter are active switches is higher than the TI and ST products, as indicated in Table I (the efficiency part). The switching technique is another consideration for microinverters. The TI, ST and UBIK products can achieve soft switching at the cost of extra component count by using the active-clamped circuit, as shown in Fig. 4 or the resonant tank as shown in Fig. 8, which in turn can decrease the high-frequency switching losses compared with the microinverters using the hard switching technique.

IV. Further Benchmarking and Future Trends of Microinverters

In addition to the above microinverters, Table II summarizes a survey of latest generation microinverters from the mainstream companies in terms of power rating, MPPT range, power factor (PF), THD, CEC efficiency, weight, power density and warranty. As presented in Table II, the power ratings of the microinverters range from 225 W to 320 W, and the efficiency and power density are up to 97.5 % and 6.85 $\mathrm{W \cdot in^{-3}}$. In addition, compared with the previous generation of products, the warranty of current products is 25 years, which matches the lifetime of PV panels.

Although these latest microinverter products have good performance, there is room for further improvements of reliability and efficiency in future microinverter products. The future trends are listed as:

1) For single-stage microinverters, novel power decoupling schemes, as the replacement of the large electrolytic capacitor, are promising solutions to extend the lifespan of the microinverter.
2) The advanced wide-bandgap devices (e.g., gallium-nitride (GaN) and silicon-carbide (SiC) power devices) can achieve low power losses, which may compensate for the switching losses at very high switching frequencies. In that case, the challenges may become the design of electromagnetic interference (EMI) filters and the thermal management.
3) In the future, a microinverter will be integrated into a PV panel, which means that the microinverter should be having a low profile. Utilizing planar magnetic components and increasing switching frequency (e.g., 1 MHz) will become increasingly popular [24].

V. Conclusion

In this paper, an overview of PV microinverters based on some selected mainstream products was presented. Through the analysis and comparison of the topological configuration

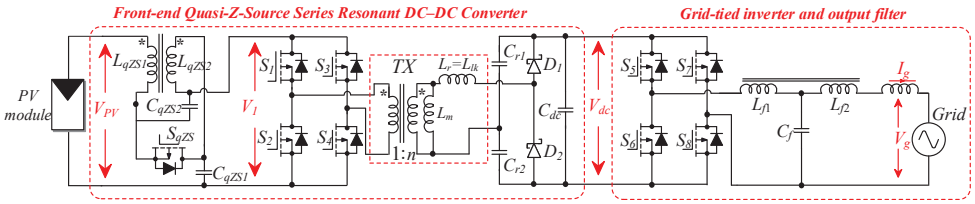

Fig. 8. Impedance-source-based PV microinverter topology [24].

TABLE I
COMPARISON OF SELECTED MICROINVERTERS.

Products	Power Rating (W)	Component Count							CEC Efficiency* Average Efficiency**
		Active Switch	High Frequency Active Switch	Low Frequency Active Switch	Magnetic Core	Copper Winding	Diode	Total	
Enphase M250	250	6	2	4	1	2	1	10	96.5%
TI Microinverter	280	6	4	2	3	4	6	19	92%
ST Microinverter	250	6	4	2	2	4	6	18	93.4%
UBIK S350	300	9	9	0	2	4	2	17	95%

TABLE II
COMPARISON OF SELECTED MICROINVERTERS.

Company	Model	Power Rating (W)	MPPT Range (V)	PF	THD	CEC Efficiency	Weight (kg)	Power Density ($W \cdot in^{-3}$)	Warranty (year)
Enphase	IQ 7X	320	25-79.5 V	0.85 leading to 0.85 lagging	-	97.5 %	1.08	4.68	25
Apsystems	YC600	600 (two module)	22-48	0.8 leading to 0.8 lagging	<3%	96.5 %	2.6	6.39	25
Chilicon Power	CP-250E	289	22-38.5	0.8 leading to 0.8 lagging	-	96 %	1.55	1.67	25
Envertech	EVT 300	300	24-42	>0.99	<3%	95 %	1.5	6.85	25
ReneSola	Replus-250A	225	22-55	>0.99	-	95 %	2	3.31	25
Darfon	G320	300	22-60	>0.99	<2%	96 %	1.3	2.83	25

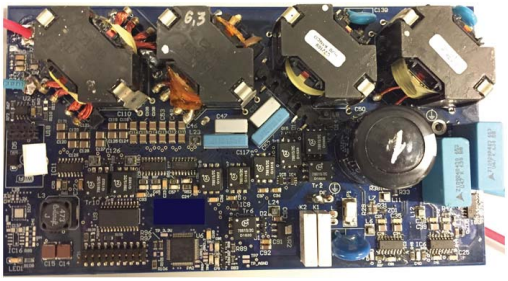

Fig. 9. Photo of the impedance-source-based PV microinverter topology [24].

and operation principles, the merits and drawbacks of these mainstream products were demonstrated. Based on the latest survey, the microinverters have superior performance in efficiency, power density and lifespan. Finally, to improve the reliability and efficiency, the future trends of microinverters are presented. Advanced power decoupling circuit and power semiconductor components will play a major role in the field of PV microinverters.

REFERENCES

[1] D. C. Martins and R. Demonti, "Photovoltaic energy processing for utility connected system," in *Proc. IEEE IECON*, vol. 2, Nov. 2001, pp. 1292–1296 vol.2.

[2] F. Appavou, A. Brown, B. Epp, A. Leidreiter, C. Lins, H. E. Murdock, E. Musolino, K. Petrichenko, T. C. Farrell, and T. T. Krader, "Renewables 2017 global status report," tech. rep., Renewable Energy Policy Network for the 21st Century (REN21), Tech. Rep., 2017.

[3] S. Kouro, J. I. Leon, D. Vinnikov, and L. G. Franquelo, "Grid-connected photovoltaic systems: An overview of recent research and emerging pv converter technology," *IEEE Ind. Electron. Mag.*, vol. 9, no. 1, pp. 47–61, Mar. 2015.

[4] S. Zengin, F. Deveci, and M. Boztepe, "Volt-second-based control method for discontinuous conduction mode flyback micro-inverters to improve total harmonic distortion," *IET Power Electron.*, vol. 6, no. 8, pp. 1600–1607, Sep. 2013.

[5] M. Keshani, E. Adib, and H. Farzanehfard, "Micro-inverter based on single-ended primary-inductance converter topology with an active clamp power decoupling," *IET Power Electron.*, vol. 11, no. 1, pp. 73–81, 2018.

[6] M. Chen, K. K. Afridi, and D. J. Perreault, "A multilevel energy buffer and voltage modulator for grid-interfaced microinverters," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1203–1219, Mar. 2015.

[7] D. Dong, M. S. Agamy, M. Harfman-Todorovic, X. Liu, L. Garces, R. Zhou, and P. Cioffi, "A PV residential microinverter with grid-support function: Design, implementation, and field testing," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 469–481, Jan. 2018.

[8] D. Meneses, F. Blaabjerg, . Garca, and J. A. Cobos, "Review and comparison of step-up transformerless topologies for photovoltaic ac-module application," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2649–2663, Jun. 2013.

[9] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep. 2005.

[10] J. Dominic, "Comparison and design of high efficiency microinverters for photovoltaic applications," Ph.D. dissertation, Virginia Tech, 2014.

[11] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, Jun. 2013.

[12] Q. Mo, M. Chen, Z. Zhang, M. Gao, and Z. Qian, "Research on a non-complementary active clamp flyback converter with unfolding dc-ac inverter for decentralized grid-connected pv systems," in *Proc. IEEE ECCE*, Sept. 2011, pp. 2481–2487.

[13] M. A. Rezaei, K. Lee, and A. Q. Huang, "A high-efficiency flyback micro-inverter with a new adaptive snubber for photovoltaic applications," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 318–327, Jan. 2016.

[14] J. Tao, V. Xue, and M. Team, "Grid-connected micro solar inverter implement using a C2000 mcu," *Texas Instruments*, 2013.

[15] R. Attanasio, "AN4070 Application Note: 250 W grid-connected microinverter," *STMicroelectronics*, 2012.

[16] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar. 2003.

[17] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *Proc. IEEE PESC*, Jun. 2008, pp. 2743–2749.

[18] D. Vinnikov, A. Chub, E. Liivik, and I. Roasto, "High-performance quasi-Z-source series resonant dcdc converter for photovoltaic module-level power electronics applications," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3634–3650, May 2017.

[19] Y. Shen, A. Chub, H. Wang, D. Vinnikov, E. Liivik, and F. Blaabjerg, "Wear-out failure analysis of an impedance-source PV microinverter based on system-level electrothermal modeling," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3914–3927, May 2019, doi: 10.1109/TIE.2018.2831643.

[20] N. David, "A sustainable solar power system for the University of Nigeria, nsukka using micro inverters."

[21] T. U. Guide. (June 2017) Digitally controlled solar micro inverter design using C2000 piccolo microcontroller. [Online]. Available: http://www.ti.com/lit/ug/tidu405b/tidu405b.pdf

[22] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.

[23] R. W. Erickson and A. P. Rogers, "A microinverter for building-integrated photovoltaics," in *Proc. IEEE APEC*, Feb. 2009, pp. 911–917.

[24] Y. Shen, H. Wang, Z. Shen, Y. Yang, and F. Blaabjerg, "A 1-MHz series resonant dc-dc converter with a dual-mode rectifier for pv microinverters," *IEEE Trans. Power Electron.*, pp. 1–1, 2018, doi: 10.1109/TPEL.2018.2876346.

[25] D. Vinnikov and I. Roasto, "Quasi-Z-source-based isolated DC/DC converters for distributed power generation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 192–201, Jan. 2011.

Conference publication 2

An Embedded Switched-Capacitor Z-Source Inverter with Continuous Input Currents

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An Embedded Switched-Capacitor Z-Source Inverter with Continuous Input Currents

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***Abstract*—This paper presents a three-phase Embedded Switched-Capacitor Z-Source Inverter (ESC-ZSI) topology with continuous input currents. In the proposed ESC-ZSI, the continuous input currents can be achieved by embedding the dc sources into the symmetrical impedance network compared with a Modified Switched-Capacitor Z-source Inverter (MSC-ZSI). A detailed operation principle analysis of the proposed topology is introduced. Moreover, the boost ratio, the voltage gain and the voltage stresses of the power switch and capacitors are carried out to highlight the advantages of the proposed topology as compared with the conventional topologies. Finally, simulation and experimental results are provided to validate the theoretical analysis.**

***Index Terms*—Impedance source inverter, Z-source inverter, embedded Z-source, continuous input current**

I. Introduction

Impedance (Z-) source inverters are being increasingly employed into power conversion applications since the invention of the Z-source inverter (ZSI) [1] and the quasi Z-source (q-ZSI) inverter [2] in the past 15 years. The traditional ZSI is shown in Fig. 1. The ZSI features that it has boost capability and inherent shoot-through protection abilities [3]–[5] compared with the traditional voltage source inverter. Moreover, the single conversion stage of the ZSIs can effectively decrease the system cost and improve the efficiency [6]–[8]. However, there are some limitations of the conventional ZSI, such as low boost factor, high voltage stresses across the capacitors and switches as well as discontinuous input current. To tackle these problems, many attempts have been made to improve the performance of the ZSIs.

The conventional ZSI has two capacitors and two inductors of identical values, as shown in Fig. 1. Notably, the high conversion ratios of the ZSIs are mainly dependent on the number of passive components and their arrangement. Fig. 2 shows a switched-inductor ZSI [9], where the switched inductor provides a voltage gain at the same shoot-through duty ratio compared with conventional ZSI. Moreover, to achieve a higher boost rating and low voltage stresses across the switching devices of the main circuit, series-connected SL or SC cells can be inserted into the topologies [10]–[12]. For instance, in [12], a modified topology with an SC impedance network (MSC-ZSI) was introduced, as shown in Fig. 3, which can achieve an even higher boost factor with a shorter shoot-through duration and a larger modulation index. However, a higher boost capability is also achieved at the expense of extra cost and volume due to the extra inductors and capacitors.

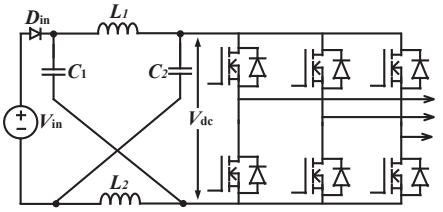

Fig. 1. Classic three-phase Z-source inverter, where V_{in} is the input DC voltage and V_{dc} is the DC-link voltage.

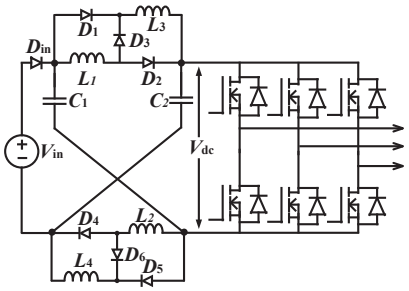

Fig. 2. Switched-inductor Z-source inverter [9].

Moreover, the dc current of the ZSI is usually discontinuous when the dc source is directly connected with the diode in the shoot-through state. To tackle this problem, the embedded ZSIs, where the dc sources are connected with inductors, were proposed in [13]–[15]. Fig. 4 shows a parallel-embedded Z-source inverter (E-ZSI), where the dc sources are embedded into the impedance network. The continuous input current can be achieved in this series connection between the dc sources and the inductors. Inspired by the above, a new Embedded Switched-Capacitor Z-source Inverter (ESC-ZSI) is then proposed in this paper. The proposed ESC-ZSI can achieve not only continuous input dc currents maintaining the same boost capability as the MSC-ZSI, but also lower stresses on the

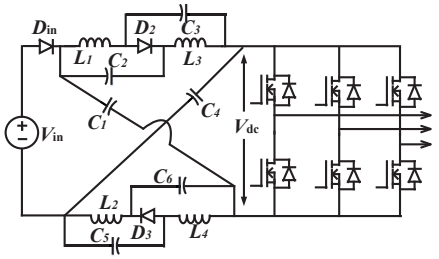

Fig. 3. Modified Switched-Capacitor Z-source Inverter (MSC-ZSI) [12].

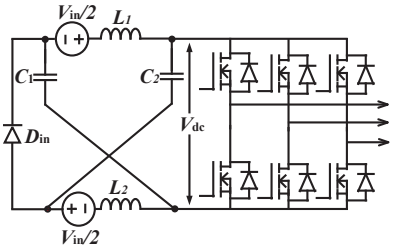

Fig. 4. Parallel-embedded Z-source inverter [13].

power devices. In Section II, the operation principle of the proposed topology is presented. Comparisons with the conventional switched impedance network and the proposed ESC-ZSI are performed, and benchmarking results are provided in Section III. Simulation and experimental results are given in Section IV, which verify the improved performance of the proposed topology in terms of continuous input dc current and lower stresses of the components. Finally, the paper is concluded in Section V.

II. Operation Principle of the Proposed ESC-ZSI Topology

The proposed ESC-ZSI is shown in Fig. 5, which has two symmetrical SC cells with embedded dc sources. The operation principle of the ESC-ZSI can be divided into two states–the shoot-through state and non-shoot-through state. The equivalent circuits of the proposed ESC-ZSI in the shoot-through state and non-shoot-through state are shown in Figs. 6 (a) and (b), respectively. It is assumed that all capacitors (or inductors) in the proposed topology are identical. Moreover, the embedded two dc sources are half of the input voltage before splitting, i.e., $0.5V_{\text{in}}$. The symmetrical topology leads to $i_{\text{L}_1} = i_{\text{L}_4}$, $i_{\text{L}_2} = i_{\text{L}_3}$, $V_{\text{C}_1} = V_{\text{C}_4}$, $V_{\text{C}_2} = V_{\text{C}_5}$, $V_{\text{C}_3} = V_{\text{C}_6}$, in which i_{L_1}, i_{L_2}, i_{L_3}, i_{L_4}, V_{C_1}, V_{C_2}, V_{C_3}, V_{C_4}, V_{C_5} and V_{C_6} are the corresponding currents through the inductor L_1, L_2 , L_3, L_4 and the voltages across the capacitor C_1, C_2, C_3, C_4 , C_5 and C_6.

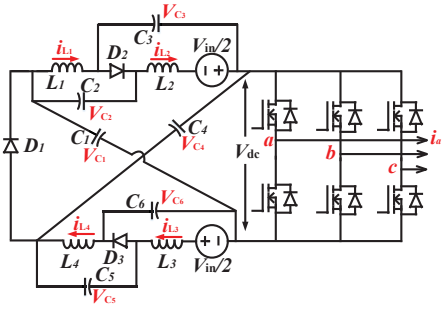

Fig. 5. Proposed three-phase switched-capacitor Z-source Inverter (ESC-ZSI).

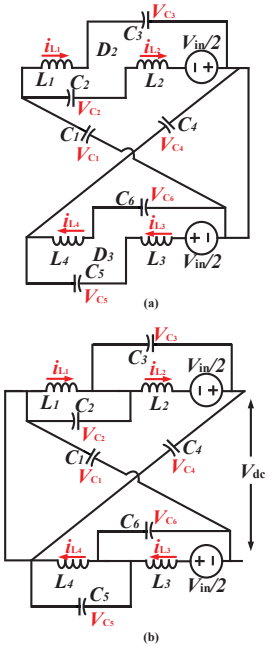

Fig. 6. Operation states for the proposed inverter (a) shoot-through state of the proposed Z-source inverter and (b) non-shoot-through state of the proposed Z-source inverter.

A. Shoot-Through State

As shown in Fig. 6 (a), three diodes D_1, D_2 and D_3 are all reverse-biased. In this case, the energy from the six capacitors is stored in the four inductors. The inductor L_1 is connected with C_1 and C_3 in series and the inductor L_2 is connected

with C_1, C_2 and one dc source in series. Then, according to the Kirchhoff's voltage law, it can be obtained that

$$V_{\text{L1-S}} = V_{\text{C}_1} + V_{\text{C}_3} \tag{1}$$

$$V_{\text{L2-S}} = V_{\text{C}_1} + V_{\text{C}_2} + V_{\text{in}} \tag{2}$$

in which $V_{\text{L1-S}}$ and $V_{\text{L2-S}}$ are the inductor voltages in the shoot-through state, and V_{in} is the dc-source voltage.

B. Non-Shoot-Through State

In the non-shoot-through state, as shown in Fig. 6 (b), three diodes are in ON state and the inductors then provide the stored energy to the ac load. During this state, the inductor voltages $V_{\text{L1-NON}}$, $V_{\text{L2-NON}}$ and the dc-link voltage V_{dc} can be represented by

$$V_{\text{L1-NON}} = -V_{\text{C}_2} \tag{3}$$

$$V_{\text{L2-NON}} = V_{\text{C}_2} - V_{\text{C}_4} + V_{\text{in}} \tag{4}$$

$$V_{\text{dc}} = V_{\text{C}_1} + V_{\text{C}_2} + V_{\text{C}_3} \tag{5}$$

It is known that the inductor average voltage in one cycle should be zero, and then applying the volt-second balance principle to all the inductors:

$$DV_{\text{L1-S}} + (1-D)V_{\text{L1-NON}} = 0 \tag{6}$$

$$DV_{\text{L2-S}} + (1-D)V_{\text{L2-NON}} = 0 \tag{7}$$

The capacitor voltages can be expressed in term of duty ratio, D and V_{in}.

$$V_{\text{C}_1} = \frac{1}{1-4D}V_{\text{in}} \tag{8}$$

$$V_{\text{C}_2} = \frac{2D}{1-4D}V_{\text{in}} \tag{9}$$

$$V_{\text{C}_3} = \frac{1-2D}{1-4D}V_{\text{in}} \tag{10}$$

The peak dc-link voltage V_{dc}^{p} and boost factor B can be derived from (8)-(10),

$$V_{\text{dc}}^{\text{p}} = \frac{2}{1-4D}V_{\text{in}} = BV_{\text{in}} \tag{11}$$

The peak output voltage V_{ac}^{p} of the inverter is expressed by

$$V_{\text{ac}}^{\text{p}} = \frac{MBV_{\text{dc}}}{2} \tag{12}$$

in which M is the modulation index. The buck-boost factor G can be expressed with respect to the modulation index as

$$G = MB = \frac{V_{\text{ac}}^{\text{p}}}{0.5V_{\text{dc}}} \tag{13}$$

TABLE I
BENCHMARKING OF SELECTED IMPEDANCE-SOURCE INVERTERS.

	ZSI [1]	MSC-ZSI [12]	E-ZSI [13]	ESC-ZSI
B	$\frac{1}{1-2D}$	$\frac{1}{1-4D}$	$\frac{1}{1-2D}$	$\frac{1}{1-4D}$
$\frac{V_s}{GV_{\text{dc}}}$	$2-\frac{1}{G}$	$\frac{4}{3}-\frac{1}{3G}$	$2-\frac{1}{G}$	$\frac{4}{3}-\frac{1}{3G}$
$\frac{V_{C_1}}{GV_{\text{dc}}}$, $\frac{V_{C_4}}{GV_{\text{dc}}}$	–	$\frac{4}{3}+\frac{2}{3G}$	–	$\frac{4}{3}-\frac{1}{3G}$
$\frac{V_{C_2}}{GV_{\text{dc}}}$, $\frac{V_{C_5}}{GV_{\text{dc}}}$	–	$\frac{2}{3}-\frac{2}{3G}$	–	$\frac{2}{3}-\frac{2}{3G}$
$\frac{V_{C_3}}{GV_{\text{dc}}}$, $\frac{V_{C_6}}{GV_{\text{dc}}}$	–	$\frac{2}{3}-\frac{2}{3G}$	–	$\frac{2}{3}+\frac{1}{3G}$

TABLE II
PARAMETERS OF THE PROPOSED ESC-ZSI IN SIMULATIONS AND EXPERIMENTS.

Parameter	Symbol	Value
dc input voltage	V_{in}	30 V
ESC-ZSI inductance	L	640 μH
ESC-ZSI capacitor	C	100 μF
Load inductance	R_f	3 mH
Load resistance	L_f	30 Ω
Switching frequency	f_s	10 kHz

III. COMPARISON OF THE PROPOSED ESC-ZSI WITH OTHER TOPOLOGIES

In order to validate the performance of the proposed ESC-ZSI, a detailed benchmarking is performed, and the results are shown in Table I. The voltage stresses are defined as the ratio of the peak dc-link voltage and capacitors voltage to the minimum dc voltage. Fig. 7 shows how the boost factor changes with the shoot-through duty ratio among the benchmarked topologies. It is further observed that in Fig. 7 the proposed ESC-ZSI and MSC-ZSI have a higher boost factor than the ZSI and the E-ZSI. In addition, the comparison of voltage gains among the selected topologies is shown in Fig. 8, where the voltage gains of the ESC-ZSI and MSC-ZSI are much higher than the E-ZSI and ZSI. Moreover, it can be seen in Fig. 9 that the power switch stress of the proposed ESC-ZSI is the same as the MSC-ZSI but much lower than the ZSI and E-ZSI for the same voltage gain. It is worth noting that the lower power rating of the switches can lead to lower cost. In addition, Fig. 10 shows that although the voltage stresses of the capacitors are not exactly the same in the MSC-ZSI and the ESC-ZSI, the sum of the stresses for all the capacitors of the ESC-ZSI is not affected in the embedded topology.

IV. SIMULATIONS AND EXPERIMENTAL TESTS

To further demonstrate the proposed ESC-ZSI, simulations and experimental tests are performed. The parameters of the inverter are shown in Table II.

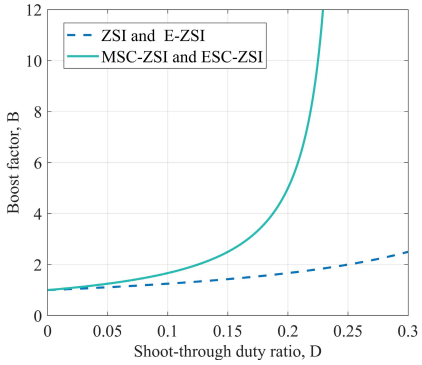

Fig. 7. Boost factor comparison of the three Z-source inverters (i.e., the ZSI, E-ZSI, and MSC-ZSI) with the proposed ESC-ZSI.

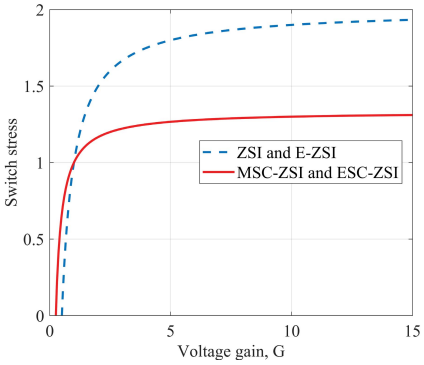

Fig. 9. The comparison of switch stress among the three Z-source inverters (i.e., the ZSI, E-ZSI, and EB-ZSI) with the proposed ESC-ZSI.

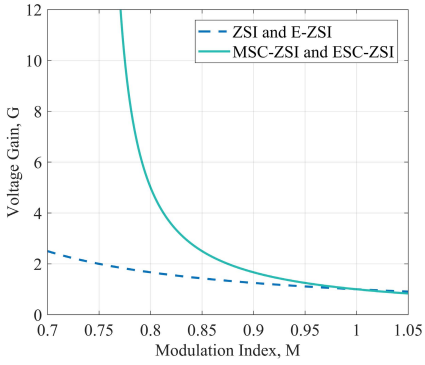

Fig. 8. Voltage gain comparison of the three Z-source inverters (i.e., the ZSI, E-ZSI, and MSC-ZSI) with the proposed ESC-ZSI.

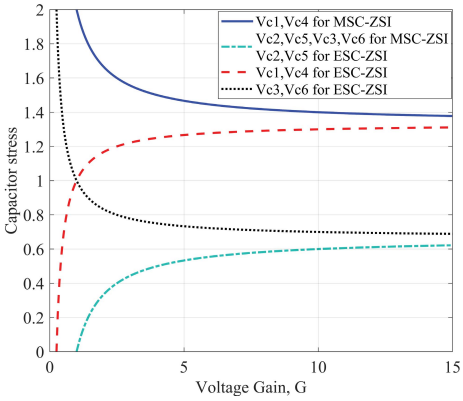

Fig. 10. The comparison of capacitor stress among the MSC-ZSI and the proposed ESC-ZSI.

A. Simulation Results

The proposed ESC-ZSI is simulated in the PLECS and MATLAB/Simulink environment using an open-loop control. The simulation results are shown in Fig. 11 under the condition $M = 0.8$ and $D = 0.175$. According to (9), the boost factor is calculated as $B = 3.33$, and thus the boosted dc-link peak voltage should be 100 V. Based on the operation principle during the shoot-through state, the inductor currents increase when the dc-link voltage is short-circuited, as shown in Fig. 11 (b). It can be seen from Fig. 5 that the two dc sources are directly connected to the inductors L_2 and L_3, so the dc input currents are also inductor, which means that the DC currents are continuous, and the peak dc-link voltage V_{dc} is almost boosted to 100 V, as expected. Moreover, as it can be seen in Fig. 11 (c), the capacitor voltages V_{C_1} V_{C_2}, V_{C_3}, V_{C_4}, and V_{C_5} are, boosted to 50 V, 17.5 V, 32.5 V, 50 V, 17.5 V, and 32.5 V, respectively. All the simulation results are in agreement with the theoretical analysis.

B. Experimental Results

An experimental setup is built up to verify the performance of the proposed ESC-ZSI and the experimental prototype is shown in Fig. 12. The experimental setup parameters are the same as simulation parameters. The switching signals are generated by a digital signal processor (DSP) TMS320F28335.

The experimental results are shown in Fig. 13. It can be seen in Fig. 13 that the currents of the inductors L_2 and L_3, that is, the currents from the dc sources are continuous. Moreover, the results show that the dc-link voltage is boosted from 30 V to 96.8 V and V_{C_1}, V_{C_2}, and V_{C_3} are maintained at 47.8 V, 16.5 V and 31.2 V, respectively. It is known that

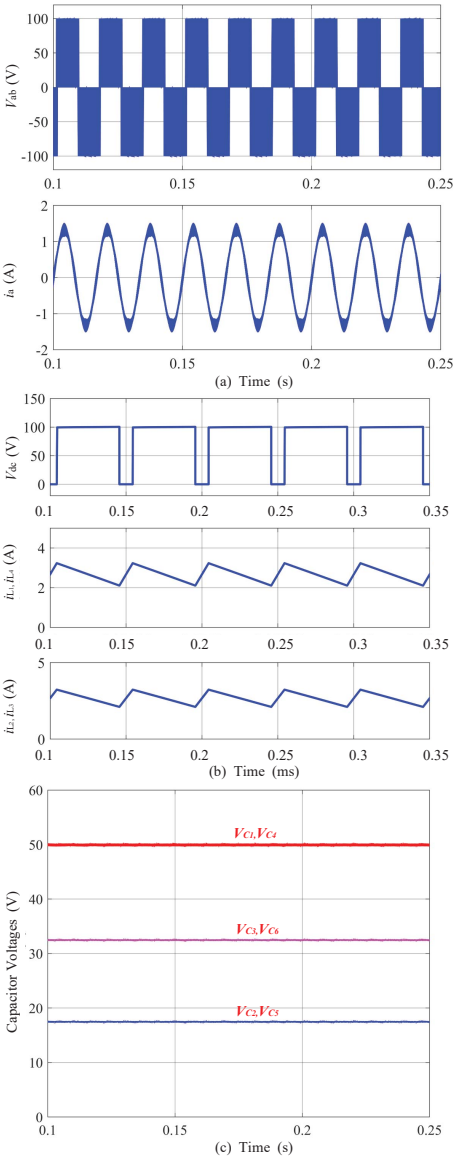

Fig. 11. Simulation results of the proposed ESC-ZSI, (a) the output leg voltage and load current in ESC-ZSI, (b) the dc-link voltage and inductor currents in ESC-ZSI, and (c) the voltages of the capacitors in the ESC-ZSI.

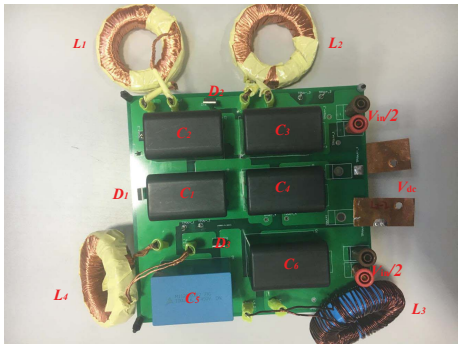

Fig. 12. Experimental prototype of the proposed ESC-ZSI topology.

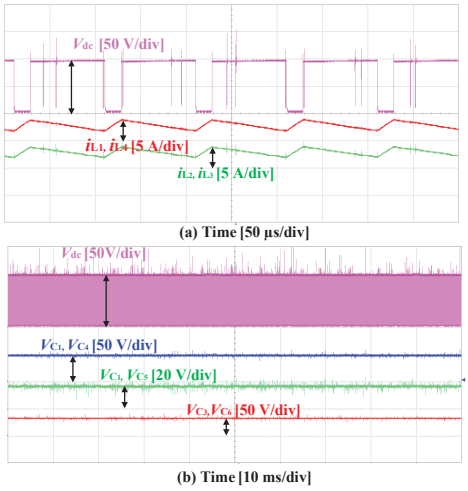

Fig. 13. Experimental results of the three-phase ESC-ZSI system: (a) the dc-link voltage V_{dc} and inductor currents i_{L_1}, i_{L_2}, i_{L_3}, i_{L_4} and (b) the dc-link voltage V_{dc} and capacitor voltages V_{C_1}, V_{C_2}, V_{C_3}, V_{C_4}, V_{C_5}, V_{C_6}.

the parasitic parameters of the inductors and capacitors, and the voltage drops of the diodes may affect the voltage gain. As a consequence, the voltages achieved in the experimental tests are slightly lower than those in the simulation cases.

V. Conclusion

In this paper, an Embedded Switched-Capacitor Z-Source Inverter (ESC-ZSI) was proposed. Compared with the traditional embedded ZSI and switched-capacitor ZSI, the current from the dc sources in the proposed topology can be continuous without affecting the boost ratio. Although two dc sources are embedded into the symmetrical topology, the stresses of the

power switch are lower than those of the MSC-ZSI and the total capacitor stresses are the same as those seen in the MSC-ZSI. Simulation and experimental tests have demonstrated that the proposed topology has a good boost capability and it is able to achieves continuous input currents.

REFERENCES

[1] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar. 2003.

[2] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *Proc. IEEE Power Electron. Sec. Conf.*, Rhodes, June 2008, pp. 2743–2749.

[3] A. Ahmad, V. K. Bussa, R. K. Singh, and R. Mahanty, "Switched-boost-modified Z-source inverter topologies with improved voltage gain capability," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 4, pp. 2227–2244, Dec. 2018.

[4] S. A. Singh, G. Carli, N. A. Azeez, and S. S. Williamson, "Modeling, design, control, and implementation of a modified Z-source integrated PV/Grid/EV DC charger/inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5213–5220, Jun. 2018.

[5] Z. Liang, S. Hu, H. Yang, and X. He, "Synthesis and design of the ac current controller and impedance network for the quasi-Z-source converter," *IEEE Trans. Power Electron.*, vol. 65, no. 10, pp. 8287–8296, Oct. 2018.

[6] E. Babaei, H. Abu-Rub, and H. M. Suryawanshi, "Z-source converters: Topologies, modulation techniques, and applicationpart i," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5092–5095, Jun. 2018.

[7] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-source networks for electric power conversion part i: A topological review," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 699–716, Feb. 2015.

[8] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "New magnetically coupled impedance (Z-) source networks," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7419–7435, Nov. 2016.

[9] M. Zhu, K. Yu, and F. L. Luo, "Switched inductor Z-source inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2150–2158, Aug. 2010.

[10] A. V. Ho, T. W. Chun, and H. G. Kim, "Extended boost active-switched-capacitor switched-inductor quasi-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5681–5690, Oct. 2015.

[11] D. Li, P. C. Loh, M. Zhu, F. Gao, and F. Blaabjerg, "Generalized multicell switched-inductor and switched-capacitor Z-source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 837–848, Feb 2013.

[12] A. Ho, S. Yang, T. Chun, and H. Lee, "Topology of modified switched-capacitor Z-source inverters with improved boost capability," in *Proc. IEEE APEC*, Mar. 2017, pp. 685–689.

[13] P. C. Loh, F. Gao, and F. Blaabjerg, "Embedded EZ-source inverters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 1, pp. 256–267, Jan. 2010.

[14] F. Gao, P. C. Loh, D. Li, and F. Blaabjerg, "Asymmetrical and symmetrical embedded Z-source inverters," *IET Power Electron.*, vol. 4, no. 2, pp. 181–193, Feb. 2011.

[15] J. Yuan, Y. Yang, P. Liu, and F. Blaabjerg, "Model predictive control of an embedded enhanced-boost Z-source inverter," in *Proc. 2018 IEEE Compel*, Jun. 2018, pp. 1–6.

Conference publication 3

Design and Analysis of a Novel Trans-inverse DC-DC Converter

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Design and Analysis of a Novel Trans-inverse DC-DC Converter

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***Abstract*—This paper explores the coupled-inductor architectures for a trans-inverse DC-DC converter. The parasitics (e.g., leakage inductance and AC resistance) will inevitably affect the performance of the coupled-inductor and thus, the entire system. More specifically, when ignoring these parasitics, the operation principle of the DC-DC converter changes and the boosting capability is degraded. Considering the application in a trans-inverse DC-DC converter, three winding arrangements are explored in detail to demonstrate their advantages and disadvantages. Finite element analysis (FEA) on the magnetics is conducted in this paper to simulate the leakage inductance and AC resistance. Finally, the performance of the trans-inverse converter with the designed winding arrangements is verified by experimental tests.**

***Index Terms*—Coupled-inductor, finite element analysis, leakage inductance, high step-up dc-dc converter**

I. Introduction

The pollution caused by the fossil fuels is increasing with the rapid industrialization. In order to reduce the adverse impact, more environmental-friendly renewable energy services such as photovolatic (PV), wind, tide waves and fuel cells are widely used in recent years. However, the output voltage from these renewable energy resources is typically so low that they cannot be directly connected to the grid/load side. To address this, high step-up DC/DC converter become essential in many renewable energy applications [1], [2]. Although the traditional boost DC-DC converters are widely employed because of the simple structure, the low boosting ratio limits further applications in high power field. To overcome this, a variety of converters have been proposed in [3]–[16].

A high voltage gain of DC-DC converters can be achieved through various configurations, e.g., the push-pull [3], half-bridge [4], full-bridge [5] and voltage multiplier cells [6], which requires high frequency transformers. Moreover, the coupled-inductor technique is an alternative to achieve high voltage gains using less components [7], [8]. The coupled-inductors DC-DC converters based on impedance-source networks, such as Γ-source [9], improved Γ-source [10], T-source [11], trans-Z-source [12], TZ-source [13], A-source [14], Σ-source [15], and Y-source [16], provide a higher voltage gain and a wider control range compared with their counterparts. In these topologies, the voltage gain is increased with a lower turn-ratio of the coupled-inductor, which significantly contributes to the overall size reduction of the converter for higher voltage gains. However, these converters require power devices with higher voltage ratings, leading to more power losses. In addition, a lower coupled-inductor turns-ratio means that the effective duty cycle to achieve the voltage boosting is narrow in practice. That is, the converter control may be challenged due to the sensitivity of the voltage gain [17]. The trans-inverse converters can achieve high voltage gains and lower voltage stresses on the switches [17], [18]. However, these converters still operate with a limited range of duty cycles (e.g., 0-0.3). To address this, a novel trans-inverse converter was proposed in [19], where the duty cycle can vary from 0 to 1, but the large input current ripples limit its applications in PV system. To tackle the aforementioned issues, a novel trans-inverse coupled-inductor Semi-SEPIC DC-DC converter, as shown in Fig. 1, was proposed in [20] with continuous input currents and high voltage gain.

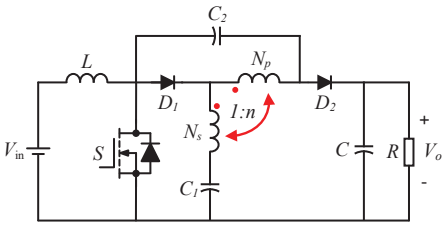

Fig. 1. Schematic of trans-inverse DC-DC converter.

It is clear that the leakage inductance will affect the performance of the trans-inverse DC-DC converter [21], as exemplified in Fig. 1. Therefore, it is necessary to achieve an optimal design of the coupled-inductors considering the effect of the leakage inductance. The accurate estimation of the coupled-inductor parasitics and the associated power losses are widely discussed in the literature [22]–[26]. Various transformer winding architectures have been explored to achieve high system efficiencies considering the leakage inductance, AC resistance and parasitic capacitance between windings. However, these solutions may not be directly applied to certain trans-inverse converters, where more attempts should be made.

In this paper, the coupled-inductor for the trans-inverse DC-DC converter (see Fig. 1) is thus analyzed and designed to minimize the leakage inductance. The rest of this paper is organized as follows. In Section II, the operation principle of the trans-inverse DC-DC topology is presented. Moreover, how the leakage inductance affects the operation principle is discussed. In Section III, the parasitics of the coupled-inductor

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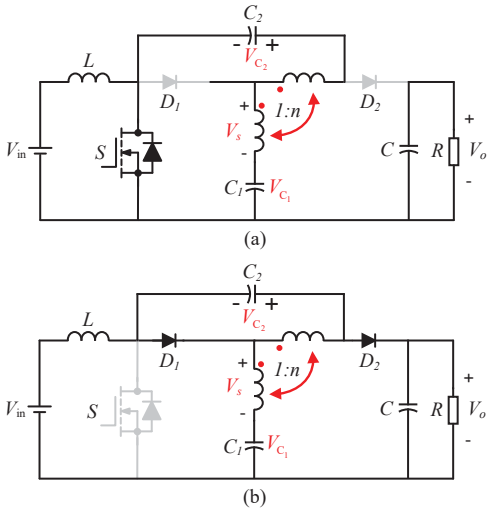

Fig. 2. Equivalent circuits of the trans-inverse converter when the switch is turned (a) ON and (b) OFF.

with three different winding architectures are explored by finite element analysis (FEA) simulations in ANSYS Maxwell. The experimental tests are given in Section IV, which verify the performance of the designed coupled-inductors. Finally, the paper concludes in Section V.

II. Operation Principle of the Trans-inverse Converter

The equivalent circuits of the trans-inverse semi-SEPIC DC/DC converter [20] are presented in Fig. 2, which includes of an input inductor (L), one active switch (S), three capacitors (C_1, C_2, C), two diodes (D_1, D_2), a leakage inductance (L_m) and a coupled inductor, where $n = N_p/N_s$ represents the turn ratio. There are two states in one switching cycle, as shown in Fig. 2. When the switch is turned ON (see Fig. 2(a)), both diodes are reverse-biased and the input source charges the input inductor L. Moreover, the source cannot transfer power to the load R due to the reverse-biased D_2, but it is powered by the output capacitor C. According to Fig. 2(a), it can be obtained that:

$$V_s = \frac{V_{C_1} - V_{C_2}}{n-1} \tag{1}$$

with V_s being the voltage across the secondary side inductance, V_{C_1} and V_{C_2} being the voltage across the capacitors C_1 and C_2.

When the switch is turned OFF and both diodes will be in the OFF state, as shown in Fig. 2(b). The stored energy in the input inductor can be delivered to the load. In this case, the voltage across the leakage inductance can be given as

$$V_s = \frac{V_{C_1} - V_o}{n-1} \tag{2}$$

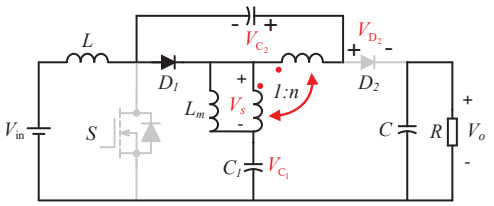

Fig. 3. : Equivalent circuit of the trans-inverse converter when the diode D_2 is turned off. (L_m is the leakage inductance)

in which V_o is the output voltage. By applying the volt-second balance principle, the voltages across C_1 and C_2, and the output voltages are obtained as

$$V_{C_1} = \left(1 + \frac{nD/(n-1)}{1-D}\right) V_{in} \tag{3}$$

$$V_{C_2} = \left(\frac{nD/(n-1)}{1-D}\right) V_{in} \tag{4}$$

$$V_o = G \cdot V_{in} = \left(\frac{1 + nD/(n-1)}{1-D}\right) V_{in} \tag{5}$$

where G is the voltage gain and D is the duty cycle.

The above analysis has been done with the assumption that the effect of the leakage inductance is neglected. If the leakage inductance is considered, the equivalent circuit for the trans-inverse converter is as shown in Fig. 3, where D_2 is turned OFF, and S is in the OFF state. The effect of the leakage inductance on the diode (D_2) voltage is shown in Fig. 4. It is observed in Fig. 4 that the voltage of D_2 has changed compared with the condition without the leakage inductance. Moreover, the boosting capability will also be degraded due to the effect of the leakage inductance. Thus, it is necessary to minimize the effect of the leakage inductance through properly designing the coupled-inductor for the trans-inverse converter.

III. Finite Element Analysis

Three winding arrangements (P/S, S/P/S, and PS/SP/S) are explored in this paper, as shown in Fig. 5, where P and S represent the primary and secondary windings with a turn ratio of 20:28. The model of the core is ETD 59/31/22/N87. The winding configurations are summarized in Table I.

In winding W_1, there is one layer with 20 turns on the primary side and two layers with 20 turns and 8 turns on the secondary side, as shown in Fig. 5(a). Moreover, for the winding W_2 in Fig. 5(b), it employs an interleaved structure, where the single primary layer is located between the two secondary layers side. A more complicated interleaved structure, as shown in Fig. 5(c) is applied in the winding W_3, where the primary and secondary windings are distributed equally in the first and second layer. The magnetomotive force (MMF) distributions for the three windings are shown in Fig. 6.

Fig. 7 shows a close-up of the magnetic field energy of the three investigated winding structures. Between the primary and secondary windings in Fig. 7(a) and (b), the magnetic

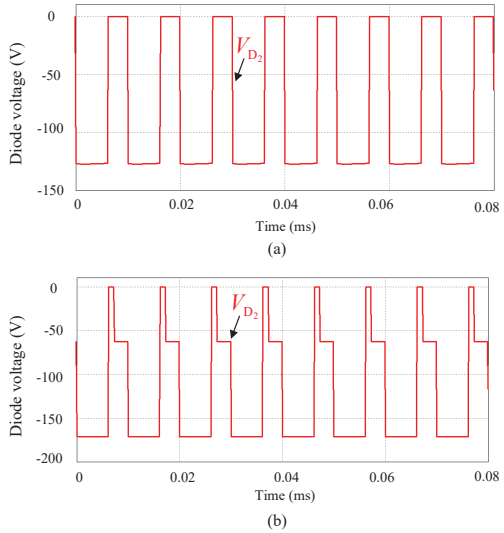

Fig. 4. Diode voltage of D_2 for the trans-inverse converter : (a) without, and (b) with the leakage inductance effect.

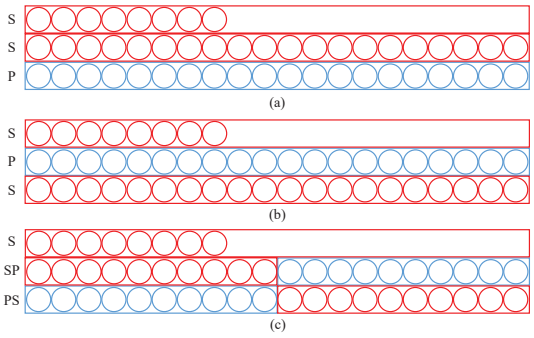

Fig. 5. Winding arrangement: (a) non-interleaved(S/P), (b) partially interleaved, and (c) fully-interleaved (PS/SP/S).

TABLE I
COUPLED-INDUCTOR ARCHITECTURES.

Design	Build-up	Primary layer and turn	Secondary layer and turn
W_1	P/S	1 and 20	2 and 20/8
W_2	S/P/S	1 and 20	2 and 20/8
W_3	PS/SP/S	2 and 10/10	3 and 10/10/8

energy is the highest in the space. In the non-interleaved winding arrangement, the MMF is the highest among all the solutions, more energy is stored between the primary and secondary windings, compared with the interleaved structures.

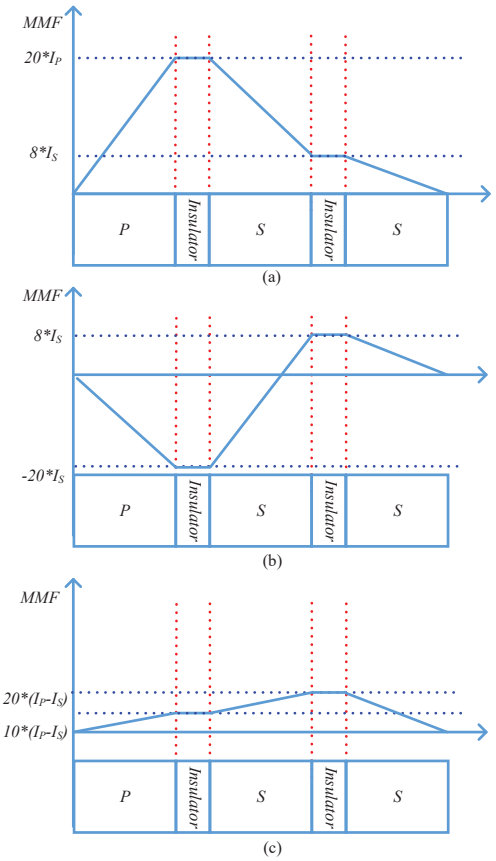

Fig. 6. Magnetomotive force (MMF) distribution for the three coupled-inductor arrangements: (a) winding W_1 (P/S), and (b) winding W_2 (S/P/S), and (c) winding W_3 (PS/SP/S).

That means, a higher leakage inductance is achieved in the non-interleaved arrangements. In the interleaved solutions, the latter is more interleaved because the primary winding is split up into two parts. More fabrication cost can be expected in this solution, as shown in Fig. 7(c). However, the highest MMF of both Fig. 7(b) and (c) are identical. However, the average MMF in Fig. 7(b) is larger than that in Fig. 7(c), which results in a higher AC resistance and leakage inductance than Fig. 7(c). In addition, the facing area between the primary and secondary in Fig. 7(b) and (c) is very close, and therefore, their stray capacitance difference is expected to be minor. This is also verified in the simulation results in Fig. 7(c) and Fig. 8(a), and it is concluded in Table II. Therefore, a "more" interleaved structure guarantees lower leakage inductance and AC losses. The trade-off between the leakage inductance and AC resistance

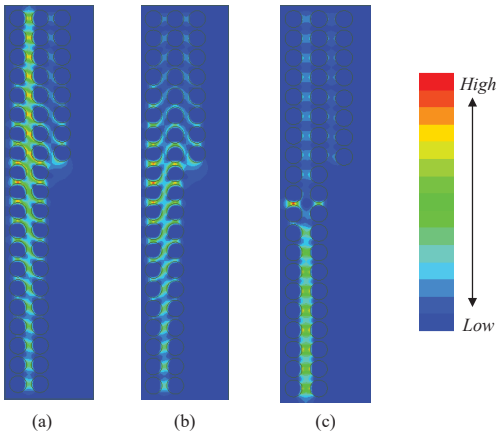

Fig. 7. Simulation plots of energy: (a) non-interleaved(P/S), (b) partially interleaved (S/P/S), and (c) fully-interleaved (PS/SP/S).

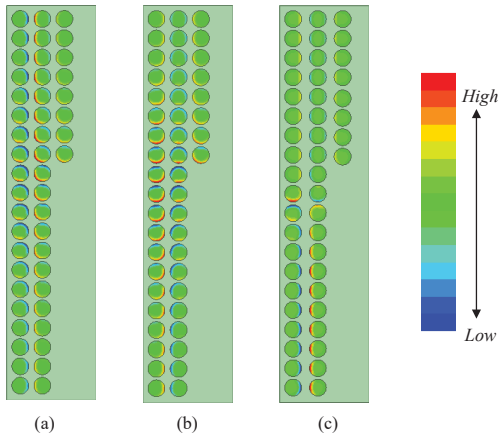

Fig. 8. Simulation plots of AC current density: (a) non-interleaved(P/S), (b) partially interleaved (S/P/S), and (c) fully-interleaved (PS/SP/S).

is further analyzed in the following.

The switching frequency of the trans-inverse converter is 100 kHz, and thus the AC resistance is simulated at 100 kHz for the three winding configurations. The current density for three winding buildups are shown in Fig. 8. Both the leakage inductance and AC resistance are calculated with the leakage magnetic field. It can be observed in Fig. 6 that the maximum MMF in the interleaved architecture is much lower than that in the non-interleaved one. Hence, the current density in the interleaved buildups (e.g., Figs. 8(b) and Fig. 8(c)) are much lower and more evenly distributed compared with the non-interleaved buildup (e.g., Fig. 8(a)). As a consequence, lower AC resistance can be achieved. Furthermore, due to the asymmetrical distribution of the winding for both primary and secondary winding, the "two-dimensional effect" appears in all the cases, where the field distortion along the horizontal direction caucuses additional resistance losses in the magnetics. Due to the more effective mixture of the primary and secondary windings, this field distortion in Fig. 8(c) is not as severe as that in Fig. 8(a) and (b). Therefore, the current density in Fig. 8(c) is distributed along the magnetic field in the vertical direction, compared with Fig. 8(a) and Fig. 8(b) with a horizontal direction component. It also decreases the AC resistance in Fig. 8(c) as well.

IV. Experimental Verification

In order to verify the above analysis, experimental tests are performed having three windings. The input voltage is 48 V and the duty cycle is set to 0.62. Based on (5), the boosted voltage should be 400 V. The parameters of the setup is shown in Table II. Furthermore, three coupled-inductors are measured, and the comparisons are shown in Table III. It can be observed in Table III that the winding W_3 has the smallest leakage inductance and ac resistance compared with the other two structures.

TABLE II
Design Parameters of the Proposed Converter.

Parameter/Decription	Value/Part Number
Power rating	150-400 W
Input/Output voltage	48/400 V
Capacitor/input inductance	100 μF/640 μH
Turn ratio	28:20 Core:B66397G0000X197
Switching frequency	100 kHz
Duty Cycle	0.62
Switch S	IPP60R099C6XKSA1
Diode D1&D2	IDP30E65D2XKSA1

TABLE III
Parameters Comparison.

	Leakage inductance		AC resistance	
	Simulation value	Measured value	Simulation value	Measured value
W_1	2.47 μH	4.3 μH	0.23 Ω	0.27 Ω
W_2	1.91 μH	3.33 μH	0.13 Ω	0.157 Ω
W_3	1.29 μH	1.8 μH	0.06 Ω	0.1 Ω

In order to verify the performance of the three windings in the trans-inverse converter, experimental tests are further carried out on a trans-inverse converter. The experimental results are shown in Fig. 9. It can be seen in Fig. 9 that the output voltages in the three windings are 366 V, 385 V and 395 V, where the winding W_3 has the best boosting capability due to its low leakage inductance and AC resistance. Moreover, it can be seen in Fig. 9 that in the windings W_1 and W_2, the diode voltage is different from that of the winding W_3, which is in agreement with the results in Fig. 4.

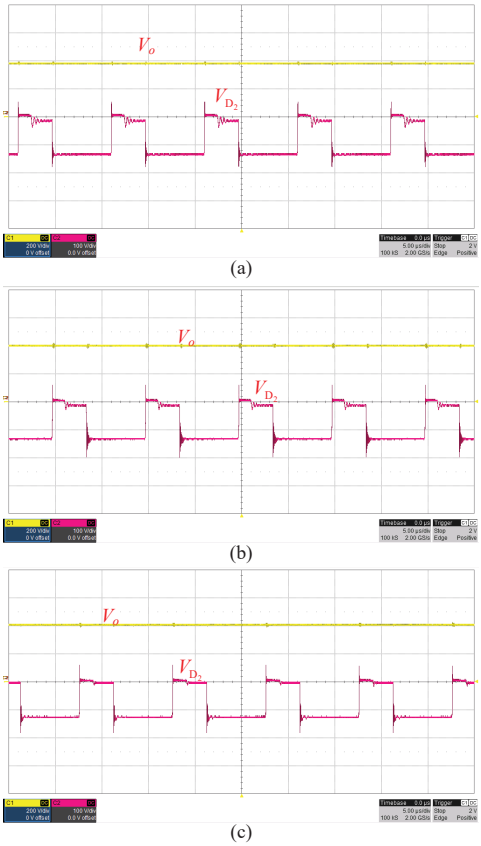

Fig. 9. Experimental results by using (a) winding W_1 (P/S), and (b) winding W_2 (S/P/S), and (c) winding W_3 (PS/SP/S) (Ouput voltage V_o (200 V/div) and Capacitor voltage V_{D_2} (100 V/div)).

V. Conclusion

In this paper, the coupled inductor architectures for a novel trans-inverse DC-DC converter were explored. It has been revealed that the performance of the trans-inverse DC-DC converter is affected by the coupled-inductor parameters. In order to optimize the design of the coupled-inductor, three winding buildups were presented. The simulation results using the FEA in ANSYS have verified that the interleaved buildups have superior performance in terms of low leakage inductance and small AC resistance. Finally, the experimental results have verified the theoretical analysis.

References

[1] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[2] F. Blaabjerg, C. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans Power Electron*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[3] S. Li, K. Xiangli, and K. M. Smedley, "A control map for a bidirectional PWM plus phase-shift-modulated pushpull DCDC converter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8514–8524, Nov. 2017.

[4] K. Xiangli, S. Li, and K. M. Smedley, "Decoupled pwm plus phase-shift control for a dual-half-bridge bidirectional DC-DC converter," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 7203–7213, Aug. 2018.

[5] A. J. B. Bottion and I. Barbi, "Input-series and output-series connected modular output capacitor full-bridge pwm DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6213–6221, Oct. 2015.

[6] B. P. Baddipadiga and M. Ferdowsi, "A high-voltage-gain dc-dc converter based on modified dickson charge pump voltage multiplier," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7707–7715, Oct. 2017.

[7] J. Yao, A. Abramovitz, and K. M. Smedley, "Analysis and design of charge pump-assisted high step-up tapped inductor SEPIC converter with an inductorless regenerative snubber," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5565–5580, Oct. 2015.

[8] K. Tseng, J. Lin, and C. Huang, "High step-up converter with three-winding coupled inductor for fuel cell energy source applications," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 574–581, Feb. 2015.

[9] P. C. Loh, D. Li, and F. Blaabjerg, "Γ-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4880–4884, Nov. 2013.

[10] W. Mo, P. C. Loh, and F. Blaabjerg, "Asymmetrical Γ-source inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 637–647, Feb. 2014.

[11] R. Strzelecki, M. Adamowicz, N. Strzelecka, and W. Bury, "New type t-source inverter," in *Proc. 2009 CPE*, May 2009, pp. 191–195.

[12] W. Qian, F. Z. Peng, and H. Cha, "Trans-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3453–3463, Dec. 2011.

[13] M. Nguyen, Y. Lim, and Y. Kim, "TZ-source inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5686–5695, Dec. 2013.

[14] Y. P. Siwakoti, F. Blaabjerg, V. P. Galigekere, A. Ayachit, and M. K. Kazimierczuk, "A-source impedance network," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8081–8087, Dec. 2016.

[15] J. J. Soon and K. Low, "Sigma-z-source inverters," *IET Power Electron.*, vol. 8, no. 5, pp. 715–723, 2015.

[16] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, S. J. Andreasen, and G. E. Town, "Y-source boost DC/DC converter for distributed generation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 1059–1069, Feb. 2015.

[17] Y. P. Siwakoti, F. Blaabjerg, and P. Chiang Loh, "High step-up trans-inverse (Tx^{-1}) DC-DC converter for the distributed generation system," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4278–4291, Jul. 2016.

[18] H. Liu, J. Wang, and Y. Ji, "A novel high step-up coupled-inductor DC-DC converter with reduced power device voltage stress," *IEEE J. Emerg. Sel. Top. Power Electron.*, pp. 1–1, 2018, doi: 10.1109/JESTPE.2018.2868769.

[19] H. Liu, F. Li, and P. Wheeler, "A family of DC-DC converters deduced from impedance source DC-DC converters for high step-up conversion," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6856–6866, Nov. 2016.

[20] A. Mostaan, J. Yuan, Y. Siwakoti, S. Esmaeili, and F. Blaabjerg, "A trans-inverse coupled-inductor semi SEPIC DC/DC converter with full control range," *IEEE Trans. Power Electron.*, pp. 1–1, 2019, doi: 10.1109/TPEL.2019.2917306.

[21] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, and G. E. Town, "Effects of leakage inductances on magnetically coupled Y-source network," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5662–5666, Nov. 2014.

[22] Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen, "Optimal design and tradeoff analysis of planar transformer in high-power DC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2800–2810, Jul. 2012.

[23] P. Thummala, H. Schneider, Z. Zhang, and M. A. E. Andersen, "Investigation of transformer winding architectures for high-voltage (2.5 kV) capacitor charging and discharging applications," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5786–5796, Aug. 2016.

[24] Z. Ouyang, J. Zhang, and W. G. Hurley, "Calculation of leakage inductance for high-frequency transformers," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5769–5775, Oct. 2015.

[25] J. Biela and J. W. Kolar, "Using transformer parasitics for resonant convertersa review of the calculation of the stray capacitance of transformers," *IEEE Trans. Ind. Appl.*, vol. 44, no. 1, pp. 223–233, Jan. 2008.

[26] Z. Shen, H. Wang, Y. Shen, Z. Qin, and F. Blaabjerg, "An improved stray capacitance model for inductors," *IEEE Trans. Power Electron.*, pp. 1–1, 2019, doi: 10.1109/TPEL.2019.2897787.

Conference publication 4

Systematic Design of Impedance Source Inverters

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Systematic Design of Impedance Source Inverters

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***Abstract*—Compared to the conventional two-stage power conversion solution, which includes a DC-DC converter and a voltage-source inverter (VSI), impedance source inverters (ISI) are increasingly developed in the last decades, where it can achieve voltage-boosting and DC-AC transformation in single-stage conversion. Hence, many efforts have been made to improve the performance of the ISIs regarding the development of novel topologies and advanced control methods. Seen from the design perspective, the performance of the ISI can be further enhanced considering the massive passive components in the ISI. However, a systematic design of impedance source inverters has not been comprehensively discussed before. Thus, a systematic design procedure to optimize the component (e.g., inductors and capacitors) is proposed in this paper in a way to maximize the performance. Especially, several design principles of the ISIs in terms of topology selection, modulation selection, switching frequency selection, and practical layout are explored. The case study further validates the effectiveness of the proposed design procedure.**

***Index Terms*—impedance source inverter, Z-source inverter, quasi-Z-source inverter, converter design**

I. Introduction

Traditional voltage source inverters (VSI) only operate in the buck condition. To address this, impedance source inverters (ISI) are increasingly developed as an effective single-stage solution in the last decade. The ISIs feature high boost capability by achieving a shoot-through state in the modulation strategy. Additionally, this single-stage solution can improve the performance of the system in terms of system cost and efficiency. As shown in Fig. 1, the Z-source inverter (ZSI) [1] and quasi-Z-source inverter (qZSI) [2] were proposed as the original impedance source inverters. However, the limited boost ratio hinders its further application. Hence, many efforts have been made to improve the performance of the ZSI/qZSI in terms of novel topologies and advanced control methods.

It is noted that increasing the boosting capability can be achieved by adding more components to the basic ZSI/qZSI network. By following this principle, the switched-inductor (SI) can be utilized to replace the inductors in the original ZSI/qZSI, thus resulting in a higher boost capability [3], [4]. In addition to the topologies based on the SI, the ZSI/qZSI can be extended by adding capacitors and diodes to the basic ZSI/qZSI network, where they are called diode-assisted ZSI (DA-ZSI) and capacitor-assisted ZSI (CA-ZSI) [5]. Although these extended ZSI/qZSI can achieve the high boost capability, they require many passive components, which lead to higher cost and larger volume of the converter [6]. To address this, several ZSI topologies with active switches were proposed [7], [8]. Compared to the ZSI/qZSI, the switched-based ZSI/qZSI have fewer passive components, but achieves the same boost capability. In addition to these non-magnetic-based impedance networks, coupled inductors and transformers are effective components to improve the performance in terms of high voltage gain [9], [10]. In certain applications, where a high voltage gain is needed, several magnetic-based impedance networks are proposed [11]–[13]. These magnetic-coupled topologies can not only achieve high boost capability but also operate under a wider control range compared to other non-magnetic-coupled topologies. However, they may suffer the negative effects due to the leakage inductance if the coupled inductors are not well designed. Therefore, it is necessary to minimize the leakage inductance by optimizing the design of the coupled inductors.

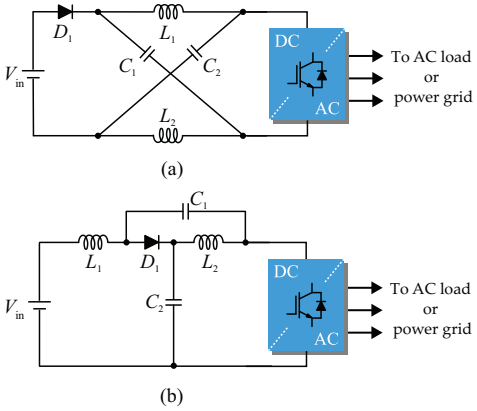

Fig. 1. Circuit schematics of impedance-source-fed three-phase inverters: (a) Z-source inverter, and (b) quasi-Z-source inverter.

Although novel topologies are increasingly developed, few have been done to address the systematic design of the ISI. Especially, certain design considerations related to the ISI has not been fully addressed yet. Inspired by the above, a systematic design procedure of the ISI is proposed in this paper. As the basis of design procedure, several design considerations in terms of topology selection, modulation selection, switching frequency selection, and practical layout optimization are also explored. The rest of the paper is organized as follows. The design considerations are presented in Section II. In Section III, the detailed design procedure is demonstrated. By following the proposed design procedure, a case study is conducted in Section IV. Finally, concluding remarks are given in Section V.

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II. Design Considerations

According to the state-of-the-art regarding the ISI, the systems based on the ISIs mainly operate for certain medium power applications ranging from hundreds to thousands of watts [1]–[18]. To maximize the performances of the ISIs, the following design principles in terms of topology selection, modulation selection, switching frequency, and practical layout optimization will be discussed.

A. Topology Selection

To choose the suitable impedance-source topology in light of certain design specifications and application scenarios, the voltage gain, input current ripple, stress across the components, and duty cycle control range should be considered. In Fig. 2, the ISIs can be divided into the following categories according to the range of the voltage gains. The basic ZSI/qZSI topologies are normally implemented for the applications where a low voltage gain (e.g., 1-2) is required. Additionally, compared to the ZSI, the qZSI is more widely used due to its characteristics of the continuous input current and lower stresses over the components. Especially, if they are applied in the single-phase PV system, the required capacitance of electrolytic capacitors for the qZSI is much lower than the ZSI, which can substantially reduce the cost [19]. Therefore, the qZSI is a promising candidate for low voltage gain applications. If application scenarios require higher voltage gains (e.g., 2-5), the switched-inductor, diode-assisted, capacitor assisted ZSI/qZSI could be further employed. Similarly, these extended impedance source networks feature different input current ripples and stresses across the components. Therefore, it is necessary to benchmark them to find a suitable candidate according to the requirements. Moreover, the ZSI/qZSI with an additional switched-boosted network could be another alternative, which operates under a wide voltage gain range. In addition to these non-magnetic-based topologies, the magnetic-coupled ZSI/qZSI could be employed for the applications, where a very high voltage gain (larger than 5) is required. By introducing the coupled inductors or transformers to the original Z/quasi Z-source networks, the boost capability is greatly enhanced [11]–[13], which makes it suitable for certain applications, such as the microinverters in the PV applications.

Additionally, a summary of different categories of impedance source topologies is presented in Table I, which addresses the main advantages, disadvantages and appropriate applications. Therefore, Table I provides a design guideline for researchers to choose the suitable topology.

B. Modulation Selection

To achieve a wider modulation range, lower voltage stress on the switches, and simpler real-time implementation, three classic PWM modulation methods (i.e., simple boost control (SBC) [1], maximum boost control (MBC) [20], and maximum constant boost control (MCBC) [21]) can be compared and selected.

In the SBC method, the shoot-through interval during the one switching period is constant and the DC current and capacitor voltage has no ripple that is related to the output frequency. However, the voltage stress across the switches is larger than the other two modulation methods. To achieve low voltage stress, the MBC is proposed and it employs shoot-through states to replace the traditional zero states. However, the variable shoot-through duty ratio introduces low-frequency ripples on the capacitor and inductors. Therefore, the prototype by using the MBC has a higher requirement of the passive components if the output frequency is not very high. The MCBC is proposed by modifying the SBC and MBC, where the MCBC makes a compromise between the SBC and the MBC. Although the voltage stress of the MCBC is higher than that of the MBC, it has lower voltage stress than that of the SBC. Moreover, there is no low-frequency ripple related to the output frequency.

C. Switching Frequency Selection

In general, the switching frequency is determined by considering the type of power devices and specific requirements of the applications. In the early stages, the ZSI/qZSI mainly employed the IGBT modules, where the switching frequency is very limited, so that the power density of the ZSI/qZSI is very low due to their large volume of the system. Therefore, the wide band gap (WBG) semiconductor devices, such as silicon carbide (SiC) and gallium nitride (GaN), provide an effective solution to improve the performance of the ZSI/qZSI. The WBG devices feature high switching frequency, low power loss, and good temperature robustness compared to the conventional silicon (Si) devices, which contributes to small passive components, high efficiency of the converter, and high power density [6].

It is known that the high switching frequency can bring about several advantages:

• Reduce the size of the magnetic components. Generally, the inductor is designed based on the peak current. Therefore, a higher switching frequency can help to reduce the magnetic component size with a reduced peak current.

• Reduce the size of the capacitors. Similarly, the capacitance is determined by the value of the ripples. By using a high switching frequency, the capacitance can be reduced due to the reduced ripples.

• Improve the power density by using these reduced components.

Moreover, the switching frequency selection is related to the power loss. And thus, in [19], the concept of critical frequency is proposed to determine the suitable switching frequency. If the switching frequency is lower than the critical frequency, the switching loss of the inverter bridge is lower than the conduction loss and the effect of switching frequency on the system efficiency is very limited. However, the power density will be very low. On the contrary, if the switching frequency is higher than the critical frequency, the switching loss dominates the whole power loss and the system efficiency will be dramatically reduced with increased switching frequency. According to the analysis from [19], the switching frequency can be optimized if the switching loss is close to the conduction loss considering the tradeoff relationship between the system efficiency and power density.

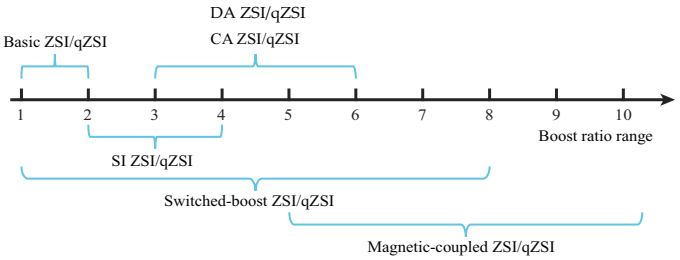

Fig. 2. The category of the impedance-source networks based on different voltage gain.

TABLE I
SUMMARY OF DIFFERENT IMPEDANCE SOURCE TOPOLOGIES AND THEIR APPLICATIONS

ZSI Type	Advantages	Disadvantages	Appropriate Application
Basic ZSI-qZSI	• Low component count • Easy to be integrated	• Discontinuous input current in ZSI • High voltage stress on capacitors • Limited voltage gain	• Motor drives application • Renewable energy applications (e.g., PV, fuel cell and wind)
DA ZSI/qZSI CA ZSI/qZSI SI ZSI/qZSI	• High voltage gain • Low voltage stress on capacitor	• High component count • Relatively heavy, bulky and costly	• Renewable energy applications (e.g., PV and fule cell) • High voltage gain applications
Switched-boost ZSI/qZSI	• High voltage gain • Low voltage stress on capacitor • Few passive component • Protect against EMI	• Complex control • Relatively heavy, bulky and costly	• Renewable energy applications (e.g., PV and fuel cell) • Hybrid electrical vehicles • Uninterruptible power supply
Magnetic-coupled ZSI/qZSI	• High boost capability • More degree of freedom • Wide control range	• High voltage spikes due to the unexpected leakage inductance • Hard to obtain the precise magnetic inductors • Relatively bulky	• High power DC supply • High voltage gain applications • Hybrid electrical vehicles • Renewable energy applications (e.g., PV and fuel cell)

D. Inductor Design

As important components in the ZSI/qZSI systems, the inductors are used to reduce the current ripple in the shoot-through state. It is noted that the inductor currents reach the maximum value at the end of the shoot-through state, where the maximum ripple current can be obtained. Moreover, based on the predefined high-frequency peak to peak current ripple (e.g., ranging from 10% to 30% of the maximum inductor current), the inductors can be calculated under a specific modulation method. In general, the inductance can be calculated by

$$L = \frac{V_L \Delta T}{\Delta I_L} \tag{1}$$

where ΔT is the shoot-through time, ΔI_L is the peak to peak current ripple, and V_L is the voltage across the inductor. The basic equation to design inductor L can be expressed as

$$L = \frac{N^2}{\Re} \tag{2}$$

where N is the number of the turns of the coil and $\Re$ is defined as magnetic reluctance, which can be obtained from the datasheet in [17].

Furthermore, the design of the magnetic components (inductors) can be optimized by building a coupled inductor in the ZSI/qZSI systems. For the conventional ZSI/qZSI, the two inductors can be built on the same core to minimize the size and weight of the inductors instead of using two separate inductors. Hence, the flux is doubled for each inductor and the inductors are expressed as

$$L = \frac{2N^2}{\Re}. \tag{3}$$

That is, the inductance is doubled. Therefore, compared to the previous non-coupled structure, the turns of the coil can be reduced to the half.

Regarding the core selection, the possible saturation behavior and abnormal temperature rise of the inductors due to the copper losses may degrade the normal operation of the converters, so the suitable core material should be selected to satisfy the requirements of electrical, magnetic and thermal design aspects [22].

Furthermore, as shown in Fig. 2, magnetic-coupled ZSI/qZSI can be applied in the applications requiring high boost ratios. However, the parasitics of the coupled inductors lead to several unexpected problems, such as high voltage spikes across the switch due to the large leakage inductance and more losses due to the AC resistance. Therefore, it is necessary to minimize the leakage inductance by optimizing the design of the coupled

inductors. In [23], different winding arrangements are explored to optimize the parasitics of the coupled inductor and the interleaved structure shows better performance in terms of low leakage inductance and small AC resistance compared to other non-interleaved structures. Hence, the leakage inductance can be minimized by applying interleaved winding structures.

E. Capacitor Design

The capacitance is another important parameter to be optimized in the ZSI/qZSI systems. The voltage rating of the capacitors can be determined according to the derived system model. Moreover, In the three-phase ZSI/qZSI systems, the capacitors are mainly used to reduce the voltage ripple to a certain range. Hence, the minimum required capacitance value can be obtained by

$$C = \frac{I_C \Delta T}{\Delta V_C} \tag{4}$$

where I_C is the current through the capacitor, and ΔV_C is the voltage ripple to maximum capacitor voltage.

Additionally, it should be noted that for the single-phase PV system based on the ZSI/qZSI, it is necessary to take into account the double-fundamental-frequency (DFF) power problem. Typically the DFF power should be absorbed by the input capacitor of the PV panels. However, due to the existence of the capacitors on the impedance network, they can also be utilized to absorb the DFF power. By building the AC equivalent model of the ZSI/qZSI, the relationship between the capacitance and the PV voltage ripple could be obtained [19], [24]. It has been validated in [24] that Z-source capacitors are more suitable to tackle the DFF problem than the input capacitors due to less electrolytic capacitors applied. In addition, compared to the ZSI, the qZSI requires less electrolytic capacitors. Therefore, the qZSI is a more promising candidate than the ZSI in terms of applications in single-phase PV systems.

F. Practical Layout Optimization

In addition to the above design considerations, layout optimization is another important design concern for impedance source inverters. Because of the shoot-through state, the operation principle of the impedance source inverters is different from the conventional voltage source converter. Therefore, different design consideration should be addressed to be applied in the impedance source inverters.

As shown in Fig. 3(a), to obtain a good layout, the stray inductance between the input dc source and inverter bridge should be as small as possible by minimizing the current loop. Under some special application scenarios that the dc source cannot be placed close to the inverter bridges, the snubber capacitor (C_{in}) could be applied to shorten the high-frequency loop. However, as shown in Fig. 3(b), the snubber capacitor cannot be placed in the ZSI due to the shoot-through state. Therefore, it may lead to high voltage spikes across the inverter switches. In addition, a similar problem may occur on the coupled-based impedance source inverters due to the large leakage inductance. To address this, several voltage clamp circuits have been applied to the impedance source inverters [25]. The detailed analysis of the voltage clamp circuits can be found in [25].

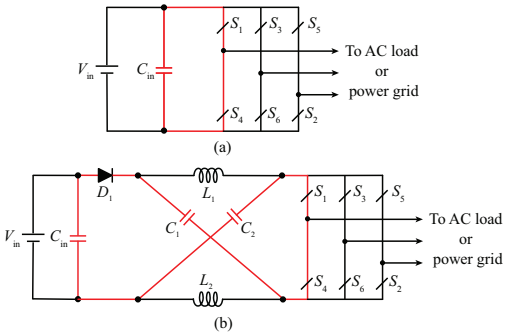

Fig. 3. High-frequency loop of conventional voltage source inverter (VSI) and Z-source inverter: (a) the VSI, and (b) the ZSI. [25]

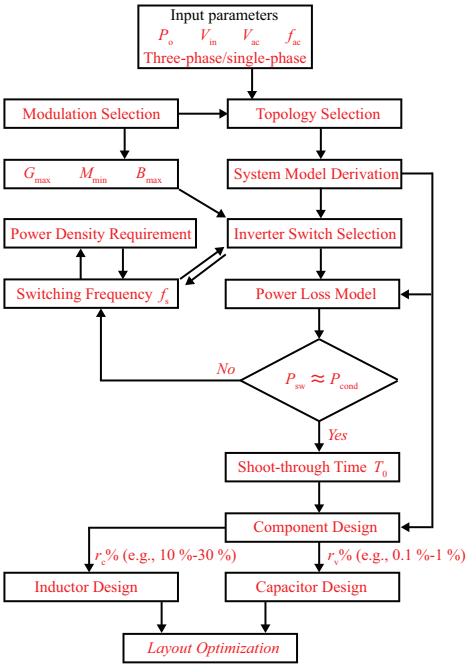

Fig. 4. Flowchart of the design procedure for impedance source inverters.

III. Design Procedure

According to the above design considerations for ISIs, a basic flowchart of the design procedure is demonstrated in Fig. 4. The following parameters are necessary for the overall design of the

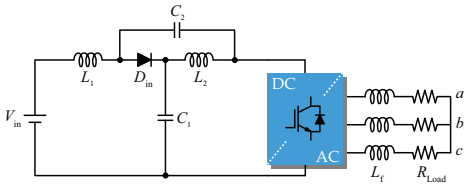

Fig. 5. Schematic of the three-phase quasi-Z-source inverter.

ISIs: P_o, rated power; V_{in}, input voltage; V_{ac}, output voltage; f_{ac}, grid frequency. Given all the input parameters specified in the flowchart, this step-by-step procedure leads to a systematic ISI design.

At first, the appropriate impedance source topology and its corresponding modulation method could be selected, taking into account the required voltage gain, input current ripple, stresses across the components and particular application scenarios. Furthermore, the maximum voltage gain $G_{\max}$ and boost factor $B_{\max}$, and minimum modulation index $M_{\min}$ can be determined based on the selected topology and modulation method. Additionally, in order to obtain the accurate specifications for the power devices and a power loss model, the system model should be derived under different operation states [19]. Then, several variables (e.g., voltage and current) related to the components can be obtained. And thus, the proper power switches can be selected based on the maximum voltage and current ratings, which can be obtained based on the system model and $G_{\max}$, $B_{\max}$ and $M_{\min}$.

Meanwhile, based on the derived power loss model, the switching frequency can be optimized by calculating the switching loss and conduction loss as stated in Section II [19]. Once the switching frequency is determined, the obtained shoot-through time T_0 can be used to design the inductor and capacitor parameters to meet the minimum requirement according to (1) and (4). Next, by following the design considerations discussed in Section II, the design optimization for inductors and capacitors can be achieved under specific application scenarios. Eventually, to implement the circuit design, optimization of the practical layout for the prototype should be performed by minimizing the high-frequency loop or adding voltage clamp circuits to the impedance networks.

IV. Case Study

By following this systematic design procedure for impedance source inverters, a case study is conducted in this part. The input parameters are summarized as: input voltage V_{in} ranges from 200 to 300 V, the system power rating P_o is 3 kW, the output is set as a three-phase grid frequency f_{ac} 50 Hz, output voltage V_{ac} 230 V system with a resistive load.

According to the input parameters, the voltage gain should be ranged between 1 to 2. And thus, the basic ZSI and the qZSI are both proper candidates as the main topology. Furthermore, due to the continuous input current and lower voltage stress across the capacitor, the qZSI is selected as the main topology, as shown in Fig. 5. And then, the maximum constant boost control is applied as the modulation method in the system due to its low voltage stress and low-frequency ripples [26]. Therefore, the required minimum voltage gain $G_{\max}$ can be calculated as

$$G_{\max} = \frac{2\sqrt{2}V_{\text{ac}}}{\sqrt{3}V_{\text{in}}} = 1.88 \tag{5}$$

Then according to the relationship among the voltage gain, modulation index and boost factor,

$$G = MB = \frac{M}{\sqrt{3}M - 1} \tag{6}$$

$$B = \frac{1}{\sqrt{3}M - 1} \tag{7}$$

Therefore, the minimum modulation index $M_{\min}$ and maximum boost factor $B_{\max}$ are calculated to 0.83 and 2.25, respectively. Furthermore, the duty cycle is calculated as

$$D = 1 - \frac{\sqrt{3}M_{\min}}{2} = 0.273 \tag{8}$$

Then the maximum voltage stress V_s on the inverter bridge is

$$V_s = B_{\max}V_{\text{in}} = 2.25 \times 200 = 450 \text{ V} \tag{9}$$

Furthermore, the maximum inductor current can be expressed as

$$I_{\text{in}} = \frac{P}{V_{\text{in}}} = \frac{3000}{200} = 15 \text{ A} \tag{10}$$

According to the power loss model presented in [19], the switching frequency can be selected as 100 kHz by considering the tradeoff between the efficiency and power density. The maximum shoot-through time T_0 is

$$T_0 = \frac{D}{f_s} = 2.73\ \mu s \tag{11}$$

In addition, the current ripple (r_i) and voltage ripple (r_v) are chosen as 20 % and 0.1 % as the acceptable values. The inductance and capacitance can be calculated by

$$L_1 = L_2 = \frac{V_L \Delta T}{I_L r_i \%} = 290\ \mu H \tag{12}$$

$$C_1 = C_2 = \frac{I_C \Delta T}{V_C r_v \%} = 34\ \mu F \tag{13}$$

Table II summarizes the system parameters by the above design procedure.

V. Conclusion

In this paper, to fill up the gap of the design principles for impedance source inverters (ISIs), a simple systematic design procedure is proposed. This procedure allows a designer to arrive at specific requirements based on certain specifications, such as boost ratio, power level, voltage and current ripple across the components, efficiency and power density. Additionally, several design considerations in terms of topology selection, modulation selection, switching frequency selection and practical layout optimization are explored in detail. Especially

TABLE II
SPECIFICATIONS OF THE ZSI SYSTEM

Parameter	Value
Inductor L_1, L_2	$290\ \mu H$
Capacitor C_1, C_2	$34\ \mu F$
Switching frequency	100 kHz
Input voltage V_{in}	$200 - 300\ V$
Output voltage V_o	$230\ V$
Rated power P_o	$3\ kW$
Filter L_f	$1.28\ mH$
Resistive load R_{load}	$18\ \Omega$

for the inductor and capacitor design, special considerations should be paid attention in view of the different application scenarios. Furthermore, a case study followed by introduced design procedure for the ISI system is conducted, which further validates the effectiveness of the proposed design procedure.

REFERENCES

[1] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar. 2003.

[2] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *Proc. IEEE PESC*, Rhodes, Jun. 2008, pp. 2743–2749.

[3] M. Zhu, K. Yu, and F. L. Luo, "Switched inductor Z-source inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2150–2158, Aug. 2010.

[4] Y. Wang, Q. Bian, X. Hu, Y. Guan, and D. Xu, "A high-performance impedance-source converter with switched inductor," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3384–3396, Apr. 2019.

[5] C. J. Gajanayake, F. L. Luo, H. B. Gooi, P. L. So, and L. K. Siow, "Extended-boost Z-source inverters," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2642–2652, Oct. 2010.

[6] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-source networks for electric power conversion part I: A topological review," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 699–716, Feb. 2015.

[7] A. Ravindranath, S. K. Mishra, and A. Joshi, "Analysis and PWM control of switched boost inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5593–5602, Dec. 2013.

[8] M. Nguyen, T. Le, S. Park, and Y. Lim, "A class of quasi-switched boost inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1526–1536, Mar. 2015.

[9] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, and G. E. Town, "Y-source impedance network," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3250–3254, Jul. 2014.

[10] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "Quasi-Y-source boost DC–DC converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6514–6519, Dec. 2015.

[11] A. Mostaan, J. Yuan, Y. P. Siwakoti, S. Esmaeili, and F. Blaabjerg, "A trans-inverse coupled-inductor semi-SEPIC DC /DC converter with full control range," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10 398–10 402, 2019.

[12] J. Yuan, A. Mostaan, Y. Yang, Y. P. Siwakoti, and F. Blaabjerg, "A modified Y-source DC/DC converter with high voltage-gains and low switch stresses," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7716–7720, 2020.

[13] Y. Shen, A. Chub, H. Wang, D. Vinnikov, E. Liivik, and F. Blaabjerg, "Wear-out failure analysis of an impedance-source PV microinverter based on system-level electrothermal modeling," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3914–3927, May 2019.

[14] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1453–1463, Jul. 2007.

[15] O. Husev, F. Blaabjerg, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, Y. P. Siwakoti, and R. Strzelecki, "Comparison of impedance-source networks for two and multilevel buck-boost inverter applications," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7564–7579, Nov. 2016.

[16] A. Ahmad, V. K. Bussa, R. K. Singh, and R. Mahanty, "Switched-boost-modified Z-source inverter topologies with improved voltage gain capability," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 4, pp. 2227–2244, Dec. 2018.

[17] M. Shen, A. Joseph, Y. Huang, F. Z. Peng, and Z. Qian, "Design and development of a 50kW Z-source inverter for fuel cell vehicles," in *Proc. CES/IEEE IPEMCC*, vol. 2, Aug. 2006, pp. 1–5.

[18] A. Battiston, J. Martin, E. Miliani, B. Nahid-Mobarakeh, S. Pierfederici, and F. Meibody-Tabar, "Comparison criteria for electric traction system using Z-source/quasi Z-source inverter and conventional architectures," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 2, no. 3, pp. 467–476, Sep. 2014.

[19] Y. Zhou, L. Liu, and H. Li, "A high-performance photovoltaic module-integrated converter (MIC) based on cascaded quasi-z-source inverters (qZSI) using eGaN FETs," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2727–2738, Jun. 2013.

[20] F. Z. Peng, M. Shen, and Z.Qian, "Maximum boost control of the Z-source inverter," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 833–838, Jul. 2005.

[21] M. Shen, Jin Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, and D. J. Adams, "Maximum constant boost control of the Z-source inverter," in *Proc. IAS Annual Metting*, vol. 1, 2004, p. 147.

[22] T. Nussbaumer, K. Raggl, and J. W. Kolar, "Design guidelines for interleaved single-phase boost PFC circuits," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2559–2573, July 2009.

[23] J. Yuan, Z. Shen, Y. Yang, A. Mostaan, and F. Blaabjerg, "Design and analysis of a novel trans-inverse DC-DC converter," in *Proc. IEEE COMPEL*, June 2019, pp. 1–5.

[24] L. Liu, H. Li, Y. Zhao, X. He, and Z. J. Shen, "1 MHz cascaded Z-source inverters for scalable grid-interactive photovoltaic (PV) applications using GaN device," in *Proc. IEEE ECCE*, Sep. 2011, pp. 2738–2745.

[25] H. Cha, Y. Li, and F. Zheng Peng, "Practical layouts and DC-rail voltage clamping techniques of Z-source inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7471–7479, Nov. 2016.

[26] Y. Li, J. Anderson, F. Z. Peng, and D. Liu, "Quasi-Z-source inverter for photovoltaic power generation systems," in *Proc. IEEE APEC*, Feb 2009, pp. 918–924.

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